IPC-2226

Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-2226

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A standard developed by IPC



IPC-2226

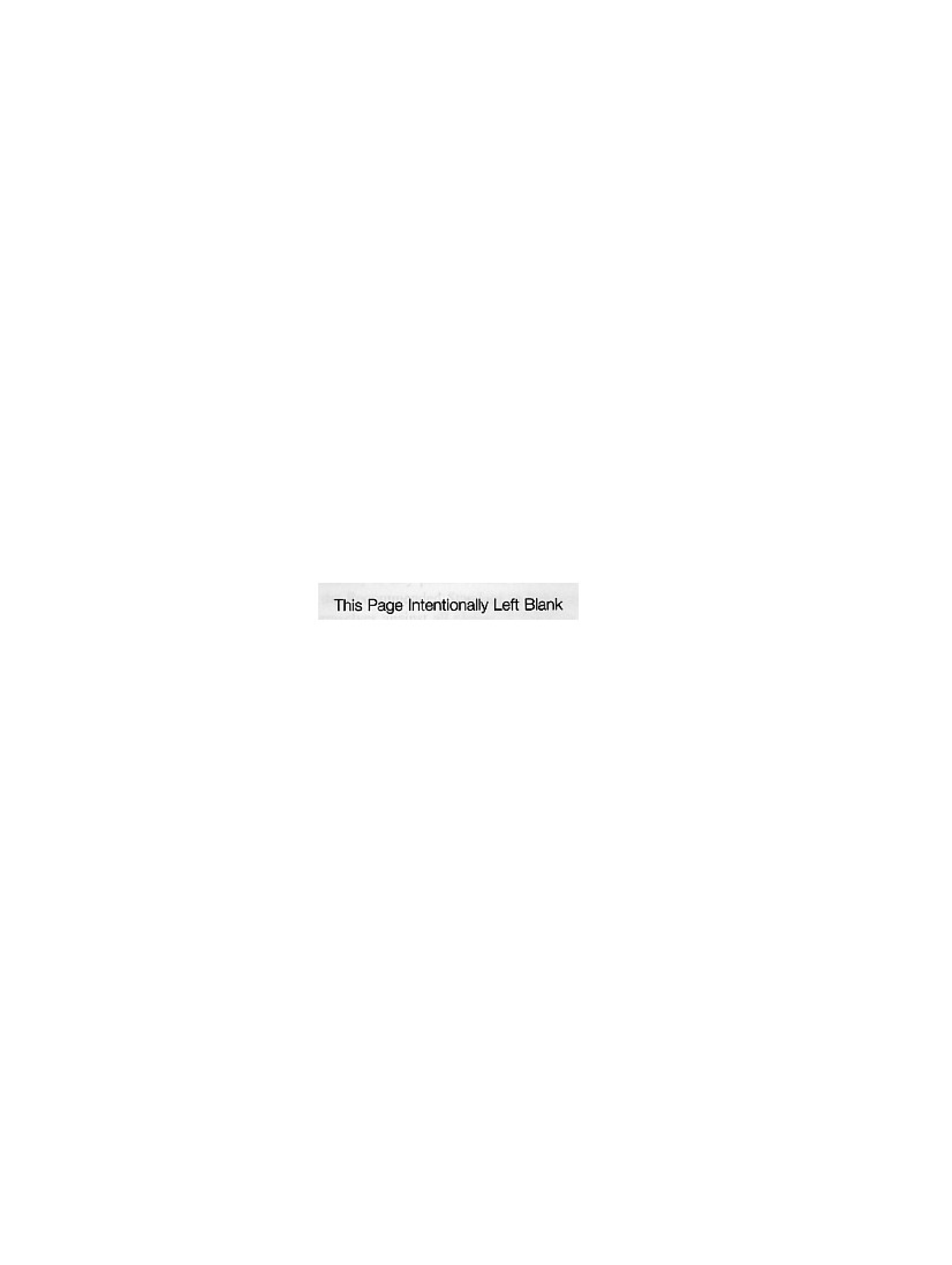
Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

Developed by the HDI Design Subcommittee (D-41) of the HDI Committee (D-40) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the HDI Design Subcommittee (D-41) of the HDI Committee (D-40) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

1 SCOPE

This standard establishes requirements and considerations for the design of organic and inorganic high density interconnect (HDI) printed boards and its forms of component mounting and interconnecting structures.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of IPC-2221. In addition, when the core material reflects requirements identified in the sectional standards (IPC-2222, IPC-2223, IPC-2224 and IPC-2225), that information becomes a mandatory part of this standard.

The standard provides recommendations for signal, power, ground and mixed distribution layers, dielectric separation, via formation and metallization requirements and other design features that are necessary for HDI-advanced IC interconnection substrates. Included are trade-off analyses required to match the mounting structure to the selected chip set.

1.2 Document Hierarchy Document hierarchy **shall** be in accordance with the generic standard IPC-2221.

1.3 Presentation All dimensions and tolerances in this standard are represented in SI (metric) units with Imperial units following as a hard conversion for reference only (e.g., 0.01 cm [0.0039 in]).

1.4 Interpretation Interpretation **shall** be in accordance with the generic standard IPC-2221.

1.5 Classification of HDI Types Classification **shall** be by category in accordance with the requirements based on end use and as stated in 1.5.1 and 1.5.2 of this standard.

1.5.1 Core Types When HDI products utilize core interconnections, the core type(s) and their materials **shall** be in accordance with IPC-2222 for rigid and IPC-2223 for flexible core interconnections. For passive or constraining core boards the materials **shall** be in accordance with IPC-2221.

1.5.2 HDI Types The design designation system of this standard recognizes the six industry approved design types (see 5.2) used in the manufacture of HDI printed boards. The designations in this section determine the HDI design type by defining the number and location of HDI layers that may or may not be combined with a substrate (core [C] or passive [P]).

For instance, an HDI printed board with two layers of HDI on one side of the core and one layer of HDI on the other side of the core would be 2 [C] 1.

The following definitions apply to all forms of HDI.

TYPE I 1 [C] 0 or 1 [C] 1 - with through vias connecting the outer layers (see 5.2.1).

TYPE II 1 [C] 0 or 1 [C] 1 - with buried vias in the core and may have through vias connecting the outer layers (see 5.2.2).

TYPE III ≥2 [C] ≥0 - may have buried vias in the core and may have through vias connecting the outer layers (see 5.2.3).

TYPE IV ≥1 [P] ≥0 - where P is a passive substrate with no electrical connection (see 5.2.4).

TYPE V Coreless constructions using layer pairs (see 5.2.5).

TYPE VI Alternate constructions (see 5.2.6).

1.6 Via Formation Via formation may be different from that considered in IPC-2221 since additional methods for via formation, in addition to drilled vias, will be used. The methods for via formation, lamination/coating and sequential layer process are covered in 9.1.1.

1.7 Design Features Figure 1-1 provides a color key to be used with all of the figures within this standard.

2 APPLICABLE DOCUMENTS

The following documents form a mandatory part of this standard and all requirements stated therein apply, unless modified in the section where they are invoked.

The revision of the document in effect at the time of solicitation **shall** take precedence over the applicable section of this document.

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

1. www.ipc.org



Figure 1-1 Color Key

IPC-CF-152 Composite Metallic Materials Specification for Printed Wiring Boards

IPC-TM-650 Test Methods Manual[2]

2.1.1 Microsectioning, Manual Method

2.1.6 Thickness of Glass Fabric

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-2221 Generic Standard on Printed Board Design

IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC/JPCA-2315 Design Guide for High Density Interconnects (HDI) and Microvias

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC/JPCA-4104 Qualification and Performance Specification for Dielectric Materials for High Density Interconnect Structures (HDI)

IPC-4412 Specification For Finished Fabric Woven From "E" Glass for Printed Board

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Structures

IPC/JPCA-6801 Terms and Definitions, Test Methods and Design Examples for Build-Up/High Density Interconnects

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-003 Solderability Test Methods for Printed Wiring Boards

J-STD-012 Implementation of Flip Chip and Chip Scale Technology

J-STD-013 Implementation of BGA and fine Pitch Technology

2.2 Underwriters Laboratories[3]

UL 746E Standard Polymeric Materials, Materials Used in Printed Wiring Boards

3 GENERAL REQUIREMENTS

3.1 Terms and Definitions Terms and definitions **shall** be as stated in IPC-T-50, IPC/JPCA-6801 and 3.1.1 through 3.1.8.

3.1.1 Microvia (Build-Up Via) A blind or subsequently buried hole that is ≤0.15 mm [0.00591 in] in diameter having a pad diameter that is ≤0.35 mm [0.0138 in] and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink-formation followed by a plating operation.

NOTE: Formed holes >0.15 mm [0.00591 in] in diameter will be referred to as vias within this standard.

3.1.2 Capture Land (Via Top Land) Land where the microvia originates; varies in shape and size based on use (i.e., component mounting, via entrance and conductor).

3.1.3 Target Land (Via Bottom Land) Land on which a microvia ends.

2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).
3. www.ul.com

3.1.4 Stacked Vias A via formed by stacking one or more microvias on a buried via that provides an interlayer connection between three or more conductive layers.

3.1.5 Stacked Microvias A microvia formed by stacking one or more microvias on a microvia that provides an interlayer connection between three or more conductive layers.

3.1.6 Staggered Vias A microvia on one layer connecting to a via on a second layer, which are offset such that the land diameters are tangential or greater. Figure 3-1 displays an example of staggered vias.

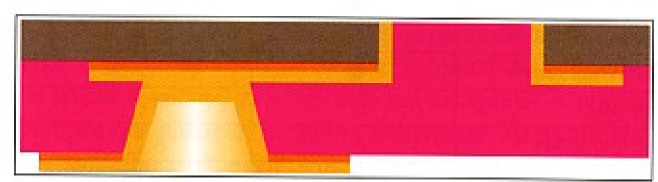


Figure 3-1 Staggered Via

3.1.7 Staggered Microvias A set of microvias, formed on two or more different layers, which are offset such that the land diameters are tangential or greater. Figure 3-2 displays an example of staggered microvias.

3.1.8 Variable Depth Microvia/Via Microvias or vias formed in one operation, penetrating two or more HDI dielectric layers and terminating at one or more different layers.

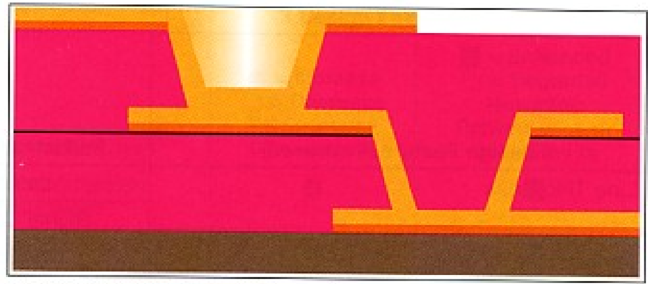


Figure 3-2 Staggered Microvias

3.2 Design Tradeoffs The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle of an HDI substrate.

Designing the physical features and selecting the materials for HDI substrates involve balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the HDI board. The tradeoff checklist (see Table 3-1) identifies the effect of changing each of the physical features or materials. Costs of the board and assembly can be and frequently are affected by these same parameters.

How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the PCB is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist

		If Design Feature is Increased	
Design Feature (Increased)	**Performance Parameter/Class**[1]	**● = Increase ○ = Decrease Performance Parameter is**	**■ = Enhanced □ = Degraded Resulting Performance or Reliability Is**
Dielectric Thickness to Ground	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	●	□
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
Line Spacing	Lateral Crosstalk/EP	○	■
	Vertical Crosstalk/EP	○	■
	Physical Size/Weight/MP	●	□
	Electrical Isolation/MY	●	■
Coupled Line	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	●	□
Line Width	Lateral Crosstalk/EP	○	■
	Vertical Crosstalk/EP	●	□
	Characteristic Impedance/EP	○	Design Driven
	Physical Size or Weight/MP	●	Design Driven
	Signal Conductor Integrity/R	●	■
	Electrical Continuity/MY	●	■

		If Design Feature is Increased	
Design Feature (Increased)	**Performance Parameter/Class[1]**	**● = Increase ○ = Decrease Performance Parameter is**	**■ = Enhanced □ = Degraded Resulting Performance or Reliability Is**
Line Thickness	Lateral Crosstalk/EP	●	□
	Signal Conductor Integrity/R	●	■
Vertical Line Spacing	Vertical Crosstalk/EP	○	■
Z_o of PCB vs. Z_o of Device	Reflections/EP	○	■
Distance between Via Walls	Electrical Isolation/R	●	■
Annular Ring (capture and target land to via)	Producibility/MY	●	■
Signal Layer Quantity	Physical Size or Weight/MP	●	□
	Layer-to-Layer Registration/MY	○	□
Component I/O Pitch	Physical Size or Weight/MP	●	□
Board Thickness	Via Integrity/R	○	□
	Via Plating Thickness/MY	○	□
Copper Plating Thickness	Via Integrity/R	●	■
Aspect Ratio	Via Integrity/R	○	■
	Producibility/MY	○	■
Overplate (Nickel -Kevlar only)	Via Integrity/R	●	■
Via Diameter	Via Plating Thickness/MY	●	■
	Via Integrity/R	●	■
Laminate Thickness (Core)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
	Via Integrity/R	○	□
	Flatness Stability/MP	●	■
Prepreg Thickness (Core)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/EP	●	□
	Via Integrity/R	○	□
Dielectric Thickness (HDI) Layer(s)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
	Via Integrity/R	○	□
	Flatness Stability/MP	○	□
Dielectric Constant	Reflections/EP	●	□
	Characteristic Impedance/EP	○	Design Driven
	Signal Speed/EP	○	Design Driven
CTE (out-of-plane)	Via Integrity/R	○	□
CTE (in-plane)	Solder Joint Integrity/R	○	□
	Signal Conductor Integrity/R	○	□
Resin T_g	Via Integrity/R	●	■
	Solder Joint Integrity/R	●	■
Copper Ductility	Via Integrity/R	●	■
	Signal Conductor Integrity/R	●	■

		If Design Feature Is Increased	
Design Feature (Increased)	Performance Parameter/Class[1]	● = Increase ○ = Decrease Performance Parameter is	■ = Enhanced □ = Degraded Resulting Performance or Reliability Is
Copper Peel Strength	Component Land Adhesion to HDI Dielectric/R	●	■
Dimensional Stability	Layer-to-Layer Registration/MY	●	■
Resin Flow	PCB Resin Voids/MY	○	■
Rigidity	Flexural Modulus/MP	●	Design Driven
Volatile Content	PCB Resin Voids/MY	●	□

1. EP = Electrical Performance, MP = Mechanical Performance, MY = Manufacturability/Yield, R = Reliability.

3.3 Design Layout The layout generation process for HDI constructions should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly, testing and those charged with thermal management. The approval of the layout by representatives of the affected disciplines will ensure that these production related factors have been considered in the design.

NOTE: Special consideration should be given to methods for ensuring the integrity of the electrical performance since the feature sizes are smaller than the capability of the presently available electrical continuity probing equipment. It is recommended that an electrical testing strategy be established for both prototype and production quantities before designing the HDI board.

3.3.1 Design Considerations The success or failure of any HDI construction depends on many interrelated design considerations, including:

- Materials selection (see Section 4).
- Manufacturing limitations are magnified for HDI substrates and restrict the capability to image, etch, form holes, plate and register. Screened or embedded components add to the complexity of the manufacturing process.
- Assembly technology used for attaching bare chips, related components and mixed technology for HDI substrates increase the complexity of the assembly operations.
- If an assembly is to be maintainable and repairable, consideration must be given to component land size and density, the selection of board and conformal coating materials and component placement for accessibility. Components with underfill typically can't be reworked.
- Finished product testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- End product assembly considerations that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement and the placement of brackets and other hardware.
- End product environmental conditions, such as ambient temperature, humidity, heat generated by the components, ventilation, shock and vibration.

3.4 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper) and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute in that they must route signals through conductors.

There are also limits to how much routing each process can accommodate. The factors that define the limits of their trace routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate.
- Number of traces that can be routed between those vias.
- Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the trace routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However, area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 3-3). See 10.4, which shows that very high I/O devices will require very dense substrate routing in order to interconnect the devices.

3.4.1 Routability Prediction Methods

3.4.1.1 Substrate Wiring Capacity Analysis After the approved schematic/logic diagrams, parts lists and end-product and testing requirements are provided and before the actual layout design is started, a wiring analysis-density evaluation should be conducted. This is based on all the parts contained in the parts list but excludes the interconnection conductors. The area usage is calculated using the

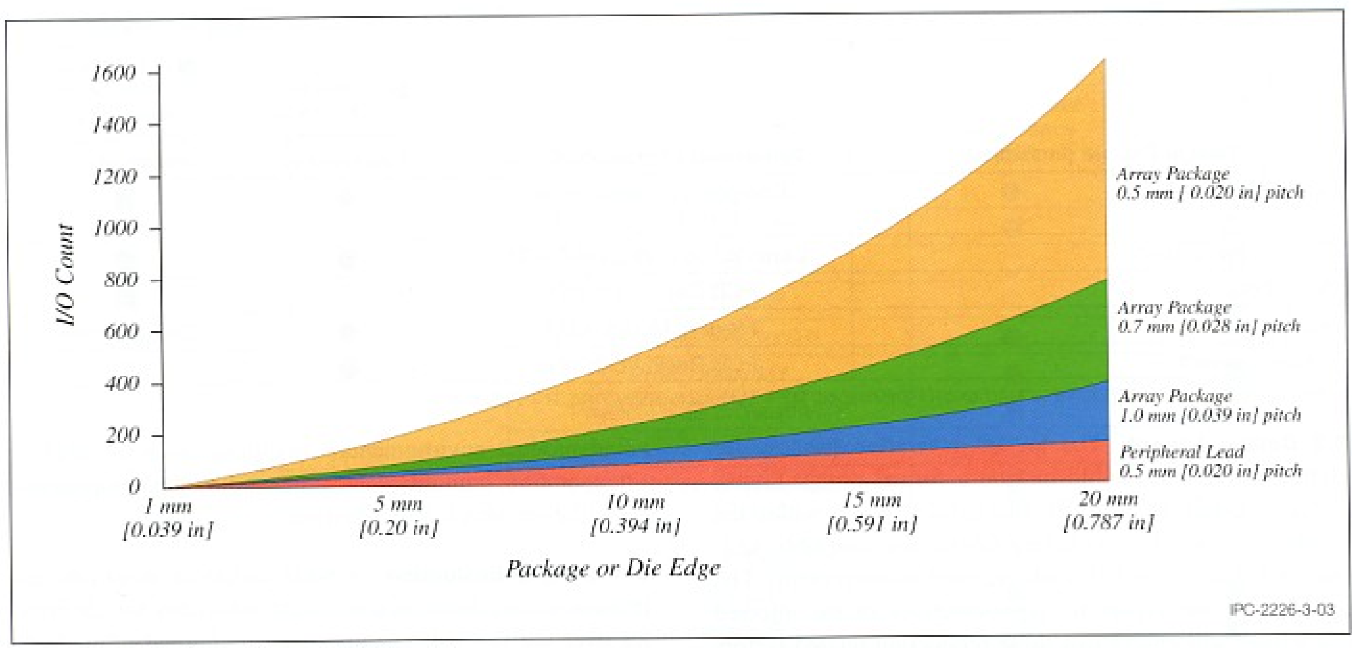


Figure 3-3 Package Size and I/O Count

largest space each part occupies, including the land pattern for mounting the components on the board and "keep out" areas for "step downs" of solder.

3.4.1.2 Wiring Capacity (W_C) Wiring capacity (W_C) is the most common definition of PCB density. This connectivity definition expresses the interconnection capability of a substrate type. It is established by determining the total length of conductors per square area of substrate (cm/cm^2 [in/in^2]) and is the total length of all conductors in all layers of the substrate divided by the area.

3.4.2 Design Basics Channel width and conductors per channel are design layout terms that refer to the distance between vias and/or component lands (channel width) and the maximum number of conductors that can be routed through each channel (conductors per channel). The feature pitch (center-to-center distance) and the size of the feature (annular ring or land size) define the channel width (see Figure 3-4 for these dimensions). The number of conductors per channel is determined by the channel width and conductor width and spacing required to meet the electrical performance of the circuit(s).

A more difficult package to include within the basic substrate design is a BGA package. The difficulty involves fan-out conductors as well as routing and via grids. Figure 3-5 provides a routing diagram as well as defining the relevant segments of the diagram.

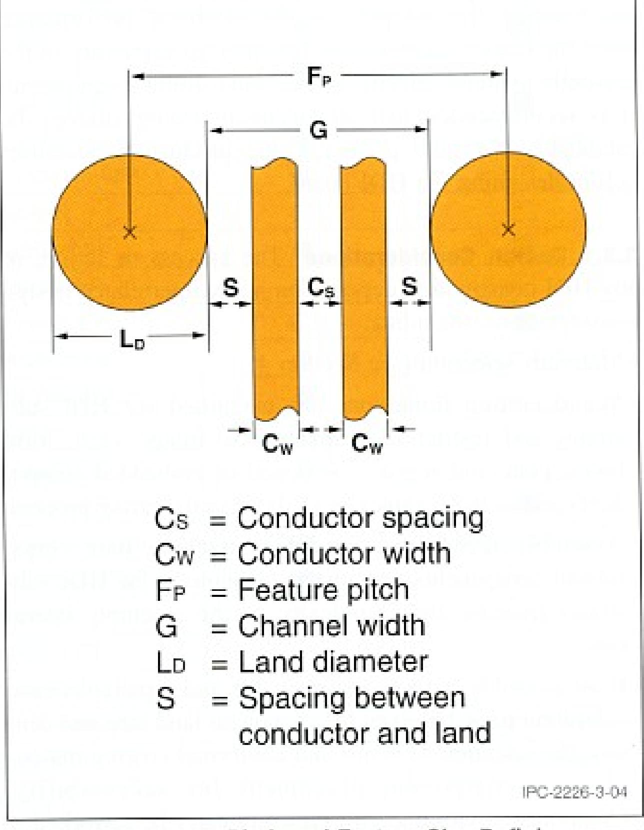


Figure 3-4 Feature Pitch and Feature Size Defining Channel Width

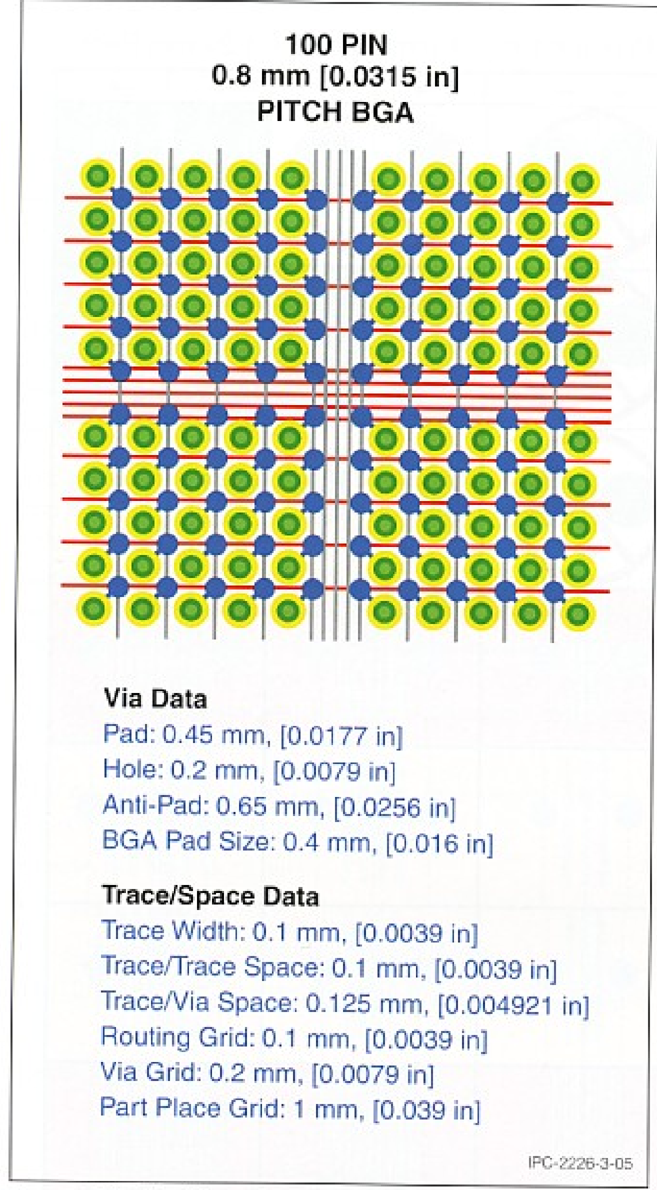


Figure 3-5 Routing and Via Grid for BGA Package

It is important to note that the land size for a microvia feature is determined, rather than simply selected, as discussed in the following.

Manufacturers successfully use a wide variety of dielectrics for microvia boards, ranging from conventional glass-reinforced epoxy to ultra-thin unreinforced materials such as resin coated copper foil. The product's end-use environment and expected operating life, plus certain needed board-level attributes (e.g., dielectric withstand voltage, resin content to fill buried vias or avoid resin starvation, etc.) may require a particular dielectric type and/or thickness for the microvia layer. However, before the microvia diameter can be determined, the designer must select the thickness and type of dielectric for the microvia layer of the board to be built.

In addition, a suitable value for the aspect ratio of the blind microvia is also needed. The aspect ratio is the ratio of the length of the hole to the diameter of the hole (L/D). Acceptable values for aspect ratio are somewhat board vendor dependent and indicative of the hole configuration the vendors can form and plate reliably and consistently. At the time this document was prepared, typical aspect ratios range from about 0.5 to 0.85, although much effort is being expanded to push this value above 1.0 (see Section 5).

Outer foil thickness should be known or estimated.

The required as-formed diameter of the microvia is calculated as shown in Equation 1.

$$\text{Microvia Diameter} = (j + f)/(A_r) \qquad \text{[Equation 1]}$$

Where:

j = Dielectric thickness on outer layer

f = Outer foil thickness

A_r = Aspect ratio

The target pad and capture pad diameters are determined by adding two annular ring widths and a fabrication allowance to the as-formed diameter of the microvia. The required fabrication allowance is a function of material behavior and fabrication process tolerances. See Section 5 for further explanation.

It is important to consider these factors before conducting the wiring assessment to ensure realistic results for the type of board to be fabricated. Also note that conductor width and spacing (and required dielectric thickness) discussed in sections 4 and 5 may not be the same for Type I and Type II boards, due to plating performed on layer 2 and layer n-1 in the Type II board (see 5.2.2).

Examples of various feature pitch and conductors per channel combinations are shown in Figure 3-6.



Figure 3-6 Feature Pitch and Conductor Per Channel Combinations

4 MATERIALS

4.1 Material Selection Material type and construction is extremely important in designing and manufacturing HDI boards.

If a core substrate is required for the HDI board, selection of the material(s) **shall** be as stated in IPC-2221. The selection of HDI materials **shall** adhere to the end product requirements. Established materials and their end product requirements are specified in IPC/JPCA-4104 which groups materials into slash sheets that are generic in nature. Due to the changing nature of this technology, there may be acceptable materials that are not yet specified in IPC/JPCA-4104.

4.1.1 HDI Material Options It is important to research the various products to choose the one best meeting the design requirements. The attributes that should be considered are:

- Moisture absorption
- Fire retardancy
- Electrical properties
- Mechanical properties
- Thermal properties

The designer and fabricator should concurrently review material selection for cost, performance and producibility.

New materials or desired combinations of materials should be reviewed with the substrate fabricator to ensure the end product will meet the requirements of the relevant certification body (e.g., UL, CSA, CE, etc.).

4.1.2 Designation System The following system identifies materials used for HDI substrates. This is a general identification system and does not in any way imply that all the permutations of properties and forms exist. Each specification sheet in IPC/JPCA-4104 outlines engineering and performance data for materials that can be used to manufacture HDI substrates. These materials include dielectric insulators, conductors and dielectric/conductor combinations.

The materials contained in IPC/JPCA-4104 represent general material categories. As new materials become available, they can be added to future revisions. Users and material developers are encouraged to supply information on new materials for review by the IPC Microvia/High Density Interconnect Materials Subcommittee (D-42). Users who wish to invoke IPC/JPCA-4104 for materials not listed **shall** list a zero for the specification sheet number (IPC-4104/0).

The designation system recognizes three general material types used in manufacturing HDI:

- Dielectric insulators only
- Conductors only
- Combinations of conductors and insulators

The first level of the designation system is the material type:

Level 1 Material Type
Dielectric Insulator = IN
Conductor = CD
Conductor and Insulator = CI

The other levels used to designate a particular material depend upon Level 1. Table 4-1, Table 4-2 and Table 4-3 illustrate the designation system for each of the material types. The designation listed in the specification sheets can be used to determine the exact material construction by first looking at the Level 1 designation (IN, CD or CI) and then looking in the correct section (4.1.2.1, 4.1.2.2. or 4.1.2.3) for that material type. These sections contain the description of the remaining designation levels with an example table to aid in deciphering the designation.

The default designations are nonphotoimageable and unreinforced. They will not be used as descriptors for simplicity (see Table 4-1, Table 4-2 and Table 4-3).

4.1.2.1 Dielectric Insulator Designations

Example: The sample from Table 4-1 will be written as IN F 1 N 1.

Note: The letter "X" **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = IN

Level 2 Form of Dielectric
Liquid = L
Paste = P
Film = F
Reinforced (Prepreg) = R
Adhesive Coated Film = C

Level 3 Photosensitivity
Nonphotoimageable = 1
Photoimageable = 2

Level 4 Reinforcement
Woven Glass = G
Nonwoven Matte Glass = M
Nonwoven Aramid = A

Table 4-1 Sample Dielectric Insulator Designation

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5
4104 / S	IN	F	1	N	1
Where S is Specification (Slash) Sheet Number	Material Type	Form of Dielectric	Photosensitivity	Reinforcement	Chemical Composition

Table 4-2 Sample Conductor Designation

IPC-4104	Level 1	Level 2	Level 3
4104 / S	CD	P	3
Where S is Specification (Slash) Sheet Number	Material Type	Form of Conductor	Type of Form

Table 4-3 Dielectric with Conductor Designations

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5	Level 6	Level 7
4104 / S	CI	F	1	N	1	CF	1
Where S is Specification (Slash) Sheet Number	Material Type	Form of Dielectric	Photo-sensitivity	Reinforce-ment	Chemical Composition	Type of Metal/ Conductor	Type of Conduction

e-PTFE (Expanded PTFE) = E
None = N
Other = O

Level 5 Chemical Composition
Epoxy = 1
Epoxy Blends = 2
Polyimide = 3
Polyester = 4
Acrylics = 5
BT Resins = 6
Cyanate Ester = 7
BCB (Benzocyclobutene) = 8
PEEK (polyetheretherketone) = 9
FEP (fluorinated ethylene propylene) = 10
LCP (liquid crystal polymer) = 11
PPE (Polyphenylene Ether) = 12
PNB (Polynorborene) = 13
Other = O

4.1.2.2 Conductor Designations

Note: The letter "X" **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = CD

Level 2 Form of Conductor
Metal Foil = F
Solution Plate = S
Printable/Paste = P
Vacuum Deposit = V
Other = O

Level 3 Type of Form
Copper = 1
Nickel = 2
Other = 3

Solution Plate (S):
Electrolytic Cu = 1
Electroless Cu = 2
Direct Plate Initiation = 3
Other Metal Plate = 4

Printable Paste (P):
Silver Particle Loaded = 1
Other Conductive Particle Loaded = 2
Transient Liquid Phase Sintering = 3
Organometallic = 4
Conductive Polymers = 5

Vacuum Deposited (V):
Evaporative = 1
Sputtering = 2
Other = 3

4.1.2.3 Dielectric with Conductor Designations

Note: The letter "X" **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = CI

Level 2 Form of Dielectric
Liquid = L
Paste = P
Film = F
Reinforced = R
Adhesive Coated Film = C

Level 3 Photosensitivity
Nonphotoimageable = 1
Photoimageable = 2

Level 4 Reinforcement
Woven Glass = G
Nonwoven Matte Glass = M
Nonwoven Aramid = A
e-PTFE (Expanded PTFE) = E
None = N
Other = O

Level 5 Chemical Composition
Epoxy = 1
Epoxy Blends = 2
Polyimide = 3
Polyester = 4
Acrylics = 5
BT Resins = 6
Cyanate Ester = 7
BCB = 8
PEEK = 9
FEP = 10
LCP = 11
PPE = 12
PNB = 13
Other = 0

Level 6 Type of Metal/Conductor
Copper Foil = CF
Copper Particle/Post = CP
Silver Particle/Post = SP
Nickel Particle/Post = NP
Alloy Particle/Post = AP
Other Particle/Post = OP

Level 7 Type of Conduction
In Plane (x-y) = 1 (e.g., Copper Foil)
Through Plane (z-axis) = 2 (Anisotropic Conductive Adhesive)
Both = 3 (e.g., Post)

4.2 Application Levels All applications for microvias require high reliability. This includes equipment where continued performance is critical, equipment downtime cannot be tolerated or the equipment is a life support item. The application levels used in IPC/JPCA-4104 slash sheets and referred to here, are:

H – Printed Circuit Board/High Density Interconnect Applications (see Figure 4-1)
I – Integrated Circuit Packaging Applications (see Figure 4-2 and Figure 4-3)
U – User Defined Applications

Application level H (see Figure 4-1) does not require moisture resistance of PCB materials testing (see IPC-TM-650, Method 2.6.16.1). Application level I (see Figure 4-1 and Figure 4-2) does not require Relative Thermal Index testing (see UL 796). User defined applications are just like application levels H or I, except the exact values and slash sheets are not defined. The values for application level U will be agreed upon between user and supplier. The intended application level is listed on each slash sheet. Certain materials may have more than one application level.

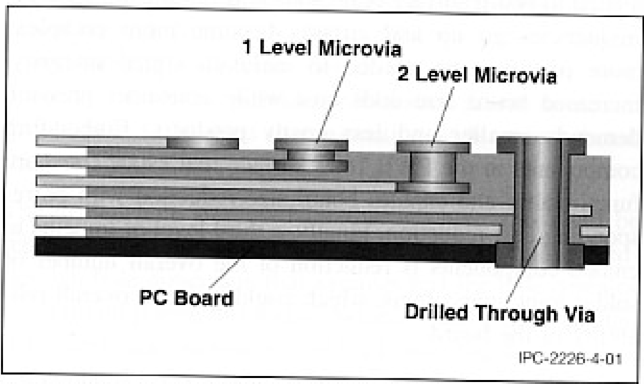


Figure 4-1 PCB-HDI/Microvia Substrate (Application H)

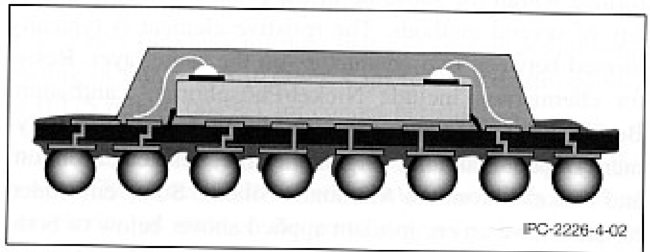


Figure 4-2 IC Carrier on HDI/Microvia Substrate (Application I)

4.3 Material Description by Type

4.3.1 Dielectric Materials

4.3.1.1 Nonphotoimageable Dielectric Materials Nonphotoimageable materials are typically supplied as a liquid, paste or dry film nonreinforced dielectric, which is applied to the sub-composite to form an insulating layer in a build-up circuit at the PCB manufacturing location. These

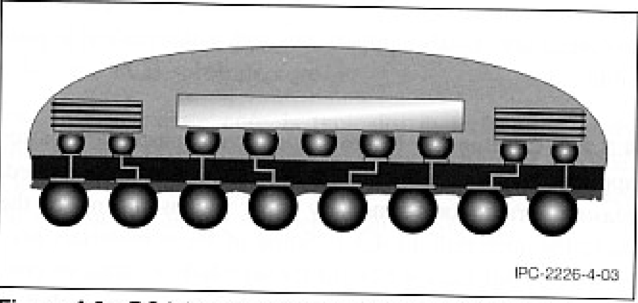


Figure 4-3 BGA Package on MCM-L Substrate Using HDI-PCB Technology (Application I)

dielectrics are suitable for via formation by LASER or mechanical methods. Some of these materials are used to fill the core board through-hole to achieve planarization.

Other materials in this group include reinforced and nonreinforced epoxies, epoxy blends, polyester, polynorborenes, polyimides, etc. (see IPC-4101).

4.3.1.2 Photoimageable Dielectric Materials Photoimageable materials are typically supplied as a liquid, paste or dry film nonreinforced dielectric, which is applied to the sub-composite to form an insulating layer in a build-up circuit at the PCB manufacturing location. These dielectrics have the capability of forming vias by photographically defined processes. Some of these materials may also be used to fill the core board through-hole to achieve planarization.

Material chemistries for this application include epoxies, epoxy blends, polyimides, etc.

4.3.1.3 Adhesive Coated Dielectric Materials These materials act as an insulator and provide the bond-ply required to adhere copper foil to the surface of a sub-composite. These materials may or may not include reinforcement. Vias are formed utilizing methods such as plasma, LASER or mechanical drilling. Materials available differ by reinforcement (e.g., woven glass, nonwoven glass, aramid, film, expanded PTFE, etc.) and chemistries involved (e.g., epoxies, polyimides, cyanate esters, acrylics, etc.).

4.3.2 Materials for Conductive Paths (In-Plane or Inter-Plane)

4.3.2.1 Conductive Foil Conductive foils are comprised of foil that are either laminated with dielectric, coated with dielectric or used as stand alone and then laminated into the structure. Foil materials are mostly copper, although other metals are possible.

4.3.2.2 Plated Conductors, Vias, Holes, Posts and Bumps These materials include various applied conductive materials that are plated (electroless and electrolytic) in vias or as bumps or posts on top of other circuitry to

make the electrical connection between layers. Plated materials are mostly copper, although other plating is possible.

4.3.2.3 Conductive Paste Conductive pastes are pastes applied into vias that are photoimaged, LASER ablated, plasma formed or formed by other means in any of the dielectric materials in 4.3.1. Some of these materials may be used to fill the core board through-hole to achieve conduction and planarity. They differ by the material that is responsible for electrical conduction. They include silver particle loaded, other metal or metal-coated particles, transient liquid phase sintering compositions organometallics and conductive polymers.

4.3.3 Materials with Dielectric and Conductive Functionality

4.3.3.1 Copper Clad Copper clad materials have copper foil (see 4.4) laminated onto one or both sides of cured (c-stage) dielectric. The typical application uses single-side clad material where the copper clad is used as the outer layer and the c-stage is bonded to the sub-composite. Vias are formed utilizing methods such as plasma, LASER or mechanical drilling. Materials available differ by reinforcement (woven glass, nonwoven glass, aramid, film and expanded PTFE) and chemistries involved (epoxies, polyimides, cyanate esters, acrylics, liquid crystal polymers, etc.).

4.3.3.2 Coated Copper Coated copper materials are comprised of copper foil, coated with a dielectric material that can be directly bonded to the sub-composite. They differ by whether they are wet processable or not. In wet processable coated copper, the vias are formed by acidic or alkaline etching or the dielectric may be made etchable by photographic definition. In nonwet processable-coated copper materials, vias are formed utilizing methods such as plasma, LASER or mechanical drilling. The materials coated are typically epoxy, polyimide or acrylic.

4.3.3.3 Anisotropically Conductive Film These materials are conductive in the z-axis and are applied as bondplies in between circuit layers to form the vertical electrical connection. They differ by the material (silver, nickel, alloy or other metals or metal-coated particles) that is responsible for electrical conduction.

4.4 Copper Foil Thinner foils are generally used by the printed board manufacturer for "fine line" designs to reduce the amount of undercutting of circuit conductors that occurs during the etch operation and meet the requirements of flip chip and chip scale packages. For multilayer constructions, the copper thickness should be specified for each layer of the board.

4.4.1 Pits, Dents and Pinholes For normal PCB materials pits, dents and pinholes are occasionally found on copper foils, but can adversely affect the quality of the finished circuit. For circuit geometries ≤75 µm [2,953 µin], it is recommended that no pits, dents or pinholes be allowed.

4.5 Embedded Electronic Components Passive components, such as resistors, capacitors and inductors, as well as active components, are referred to as embedded components when placed within the substrate of the printed wiring board. A wide variety of materials and methods can be used when embedding these circuit functions within the PCB and there are a number of reasons why designers would want to embed components within an HDI PCB. The primary reason is related to circuit function. In digital circuits, clock rates drive the signal rise time. In analog circuits bandwidth drives signal rise times. As signal rise times decrease and corresponding frequencies increase, the lead inductance associated with discrete, surface mount components begins to degrade circuit function. Moving the component from the surface of the PCB into the substrate reduces the lead inductance and parasitic capacitance. Secondary considerations for embedding components are related to board surface real estate and subsequent cost. As frequencies go up and circuits become more complex, more passives are needed to maintain signal integrity. Increased board size adds cost while consumer pressure demands smaller and less costly products. Embedding components in the PWB frees surface real estate for more functionality and enables board size reduction with corresponding cost reduction. Finally, a third level of impetus to embed components is reduction of the overall number of solder joint connections, which could improve overall reliability of the board.

4.5.1 Embedded Resistors Embedded resistors are formed within the substrate of the printed wiring board by any of several methods. The resistive element is typically formed between two conductors on the same layer. Resistor chemistries include Nickel/Phosphorus, Lanthanum Boride, Mixed Metal in Organic Matrix, Conductive Polymer, Doped Platinum, Organometallic, Nickel/Chromium and Nickel/Chromium/Aluminum Silicon. Some embedded resistors have an encapsulant applied above, below or both. The encapsulant materials are typically epoxy based.

4.5.2 Embedded Capacitors Embedded capacitors are formed within the substrate of the printed wiring board by any of several methods. There are two distinct differences among embedded capacitor materials. One type is in the form of an innerlayer laminate comprised of a dielectric core having copper or other form of conductor on both sides of the core. The copper or other form of conductor on each side of the dielectric forms the two plates of the capacitor. The other type is dielectric applied in discrete

locations on a layer with the copper or other conductor initially existing on that layer forming one plate of the capacitor and a copper or silver based paste applied as the second electrode. Some embedded capacitors have an encapsulant applied.

4.5.3 Embedded Inductors Embedded inductors are typically made by imaging the copper on one or more layers within the printed wiring board in spiral patterns. Inductors are also made by applying a ferromagnetic material above, below or between the spiral conductor patterns.

5 MECHANICAL/PHYSICAL PROPERTIES

5.1 HDI Feature Size The typical feature sizes for HDI products are in accordance with Table 5-1. Characteristics identify microvia diameter, conductor definition, total board/core thickness and via hole to board thickness aspect ratios.

5.1.1 Minimum Hole Sizes for Plated-Through Hole Vias Table 5-2 provides information on the minimum drilled hole size to be used in conjunction with various board thicknesses. In order to meet the performance requirements of the various classes of equipments, the plated-through hole size to board thickness aspect ratio for plated-through hole vias should be in accordance with Table 5-1. Table 5-2 provides information on the minimum drilled hole to be used in conjunction with various board thicknesses.

The drilled hole size used for through hole vias **shall** be represented on the master drawing as the maximum plated-through hole dimension that assumes that the hole contains a minimum plating thickness. No minimum plated-through hole dimension should be specified since the through-hole via contains no component lead or pin and could theoretically be plated shut. Thus, a master drawing call out of 0.0 mm -0.2 mm [0.0 in - 0.0079 in] diameter reflects drilling a 0.25 mm [0.00984 in] hole that can contain a minimum plating of 0.025 mm [0.000984 in] to a maximum plating of 0.125 mm [0.004921 in] copper per side.

In addition, Table 5-2 contains a letter code in each of the boxes. This letter code reflects the producibility level of complexity in each of the particular hole size to aspect ratios.

5.2 Construction Types The construction types detailed in 5.2.1 through 5.2.6 identify the characteristics of the six HDI types.

NOTE: Asymmetric build-ups dramatically increase the potential for warp and twist.

5.2.1 HDI Type I Constructions - 1 [C] 0 or 1 [C] 1 This construction describes an HDI in which there are both microvias and conductive vias used for interconnection.

Type I constructions describe the fabrication of a single microvia layer on either one (1 [C] 0) or both (1 [C] 1) sides of a PCB substrate core.

The PCB substrate core is typically manufactured using conventional PCB techniques and may be rigid or flexible. The substrate can have as few as one circuit layer or may be as complex as any number of innerlayers.

The example in Figure 5-1 shows a 1 [C] 1 Type I construction. In this construction a single layer of dielectric material is placed on both sides of the core substrate. Microvias are formed connecting layer 1 to layer 2 and layer n to layer n-1. A through-hole is then formed connecting layer 1 to layer n. The microvias and holes are then metallized (they can be filled with conductive material if required), layer 1 and layer n are circuitized and fabrication is completed. Table 5-1 includes typical feature sizes for these constructions.

5.2.2 HDI Type II Constructions - 1 [C] 0 or 1 [C] 1 Type II constructions describe an HDI board in which there are plated microvias, plated buried vias and may have PTHs used for surface-to-surface interconnection. The buried vias may be prefilled with a conductive/nonconductive paste or partially or completely filled with dielectric material from the lamination process.

The example in Figure 5-2 shows a 1 [C] 1 Type II construction, which has two through vias in the core substrate formed prior to applying the HDI dielectric layers. Both vias connect layer 2 to layer n-1. The via on the right is filled with a conductive paste. The via on the left is filled with HDI dielectric.

Microvias on layer 1 and layer n make the connection to the conductors on layer 2 and layer n-1, making the connection with the core vias. If needed, Type II constructions can also have vias formed connecting layer 1 directly to layer n (this is displayed in Figure 5-2).

Table 5-1 includes typical feature sizes for these constructions.

5.2.3 HDI Type III Constructions - ≥2 [C] ≥0 Type III constructions describe an HDI board in which there are plated microvias, plated buried vias and may have PTHs used for surface-to-surface interconnection. The buried vias may be prefilled with a conductive/nonconductive paste or partially or completely filled with dielectric material from the lamination process. Caution: Unbalanced constructions may result in warp and twist.

Type III constructions are distinguished by having at least two microvia layers on at least one side of a substrate core.

The example in Figure 5-3 shows a substrate core that has been applied with a dielectric layer on each side. Microvias have been formed connecting layer 2 to layer 3 and layer n

Table 5-1 Typical Feature Sizes for HDI Construction, µm [mil]

	ASPECT RATIOS	Level A	Level B	Level C
	Microvia plating aspect ratio	≤0.5:1 (k + j) / a	>0.5:1 to 1:1 (k + j) / a	>1:1 (k + j) / a
	Through via hole aspect ratio	≤5:1 (2k + Board Thickness) / h	>5:1 to 9:1 (2k + Board Thickness) / h	>9:1 (2k + Board Thickness) / h
	Buried via aspect ratio	≤5:1 (2r + q) / o	>5:1 to 9:1 (2r + q) / o	>9:1 (2r + q) / o
Symbol	**Feature**	**Level A**	**Level B**	**Level C**
a	Microvia diameter at target land (as formed, no plating)	102 µm [4 mil]	76 µm [3 mil]	51 µm [2 mil]
b	Microvia diameter at capture land (as formed, no plating)	152 µm [6 mil]	127 µm [5 mil]	76 µm [3 mil]
c	Microvia target land size = [(a + 2x annular ring) + FA [(1)]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for c =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4 mil]
d	Microvia capture land size = [(b + 2x annular ring) + FA [(1)]]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for d =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4mil]
s	Internal conductor trace width	127 µm [5 mil]	75 µm [3 mil]	50 µm [2 mil]
t	Internal conductor spacing	127 µm [5 mil]	100 µm [4 mil]	50 µm [2 mil]
e	External conductor trace width	127 µm [5 mil]	75 µm [3 mil]	45 µm [1.77 mil]
f	External conductor spacing	127 µm [5 mil]	100 µm [4 mil]	45 µm [1.77 mil]
g	Through via land size = [(h + 2x annular ring width) + FA [(1)]]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
h	Through via diameter (as formed, no plating)	See Table 5-2	See Table 5-2	See Table 5-2
i	Minimum through via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
j	Dielectric thickness (HDI blind microvia layer) [(2)]	64	64 µm [2.5 mil]	<50 µm [2 mil]
k	External Cu foil thickness (if Cu foil utilized)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
m	Minimum blind microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
m'	Minimum buried microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
n	Minimum buried via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
o	Buried via diameter (as formed, no plating)	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4
p	Buried via land size = [(o + 2X annular ring) + FA [(1)]]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
q	Buried via core thickness (excluding outermost conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
r	Buried via Cu foil thickness (outermost layer)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
u	Core board thickness (excluding conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
	Staggered via pitch	(p+c)/2	(p+c)/2	(p+c)/2

1. F.A. = Fabrication Allowance which considers production master tooling and process variations required to fabricate printed boards.
2. Measured from top surface of Layer 2 Cu to bottom surface of Layer 1 Cu.

Table 5-2 Minimum Drilled Hole Size for Plated-Through Hole Vias

Board Thickness	Class 1	Class 2	Class 3
<1.0 mm [0.0394]	Level C 0.15 mm [0.00591 in]	Level C 0.2 mm [0.0079 in]	Level C 0.25 mm [0.00984 in]
1.0 mm to 1.6 mm [0.0394 in to 0.0630 in]	Level C 0.2 mm [0.0079 in]	Level C 0.25 mm [0.00984 in]	Level B 0.3 mm [0.012 in]
1.6 mm to 2.0 mm [0.0630 in to 0.0787 in]	Level C 0.3 mm [0.012 in]	Level B 0.4 mm [0.016 in]	Level B 0.5 mm [0.020 in]
>2.0 mm [0.0787]	Level B 0.4 mm [0.016 in]	Level A 0.5 mm [0.020 in]	Level A 0.6 mm [0.024 in]

Note: If the copper-plating thickness in the hole is greater than 0.03 mm [0.0012 in], the hole size can be reduced by one class.

to layer n-1. The top layer is then metallized, a second dielectric layer is applied to it and microvias are formed connecting layer 1 to layer 2. A PTH is then formed, connecting layer 1 to layer n and the microvias and PTH are then metallized or filled with a conductive material. Layer 1 and layer n are then circuitized and fabrication is completed.

Table 5-1 includes typical feature sizes for these constructions.

5.2.3.1 Type III HDI with Stacked Vias and Stacked Microvias Figure 5-4 displays an example of a Type III HDI board with stacked microvias.

Table 5-1 gives typical feature sizes for these constructions.

5.2.3.2 TYPE III HDI with Staggered Vias and Staggered Microvias Figure 5-5 displays a very complex HDI board, which utilizes staggered vias, a PTH, microvias filled with conductive paste and several HDI layers.

Table 5-1 gives typical feature sizes for these constructions.

5.2.3.3 TYPE III HDI with Variable Depth Blind Vias Figure 5-6 displays an example of a Type III HDI board with variable depth blind vias.

5.2.4 HDI Type IV Constructions - ≥1 [P] ≥0 Type IV constructions describe an HDI in which the microvia layers are used over an existing predrilled passive substrate. Additional microvia layers can be added sequentially. The core substrate is usually manufactured using conventional PCB techniques. The function of the core is passive, yet it may be used for thermal, CTE management or shielding (the core doesn't perform an electrical function).

The example in Figure 5-7 shows a passive substrate core that has been applied with a dielectric layer on each side. That layer is then plated and a second layer is applied to each side. Microvias are then formed connecting layer 1 to layer 2 and layer n to layer n-1. A via is then formed, which passes between a preformed opening in the core, connecting layer 1 to layer n.

Table 5-1 includes typical feature sizes for these constructions.

5.2.5 Type V Constructions (Coreless) - Using Layer Pairs Type V constructions describe an HDI in which

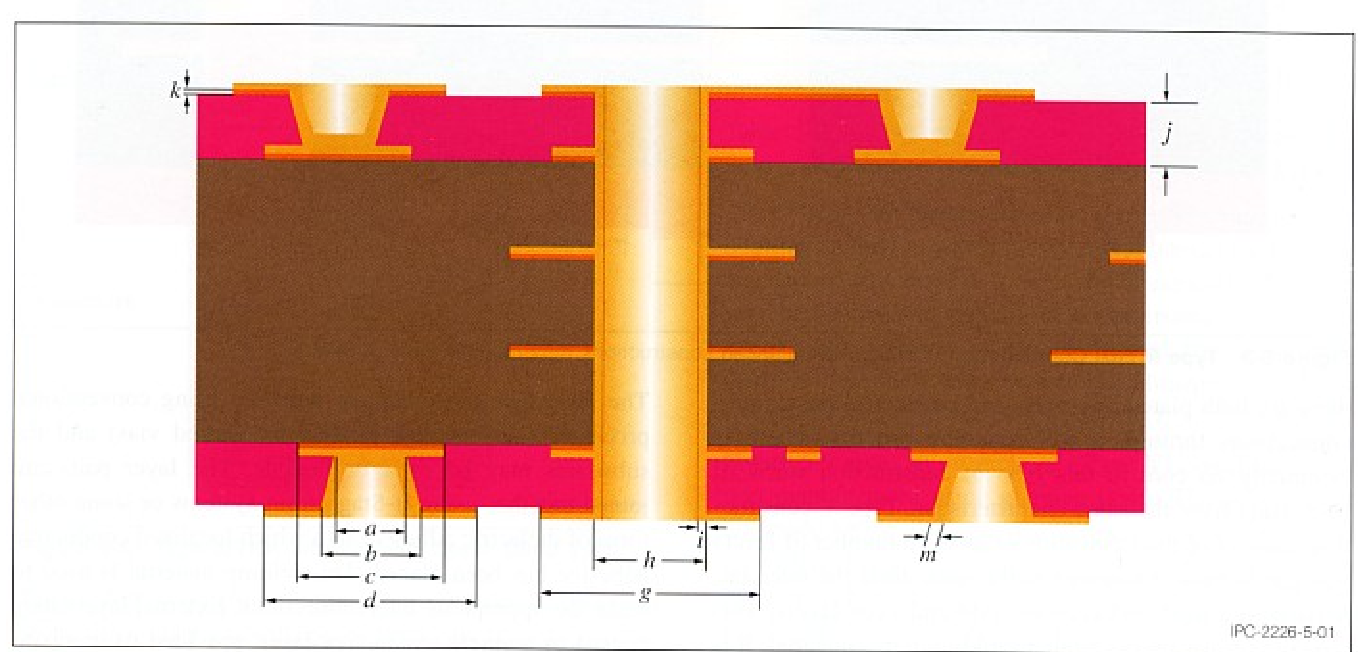


Figure 5-1 Type I HDI Construction

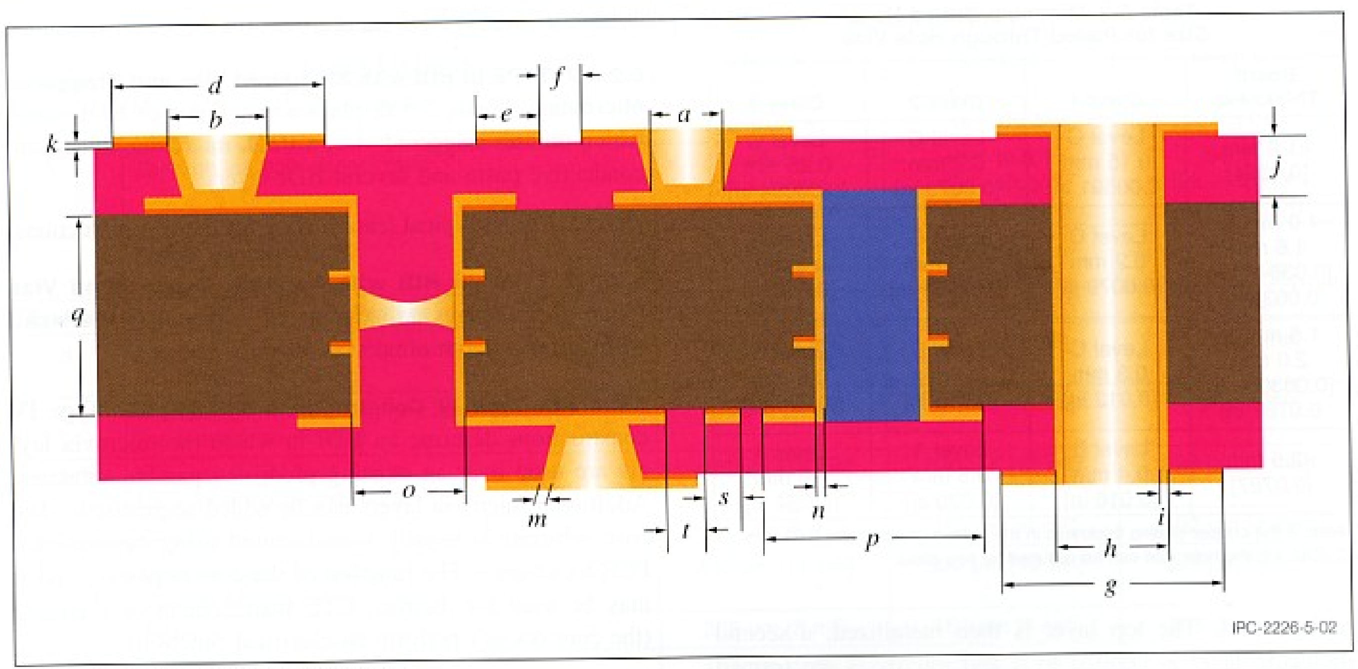


Figure 5-2 Type II HDI Construction

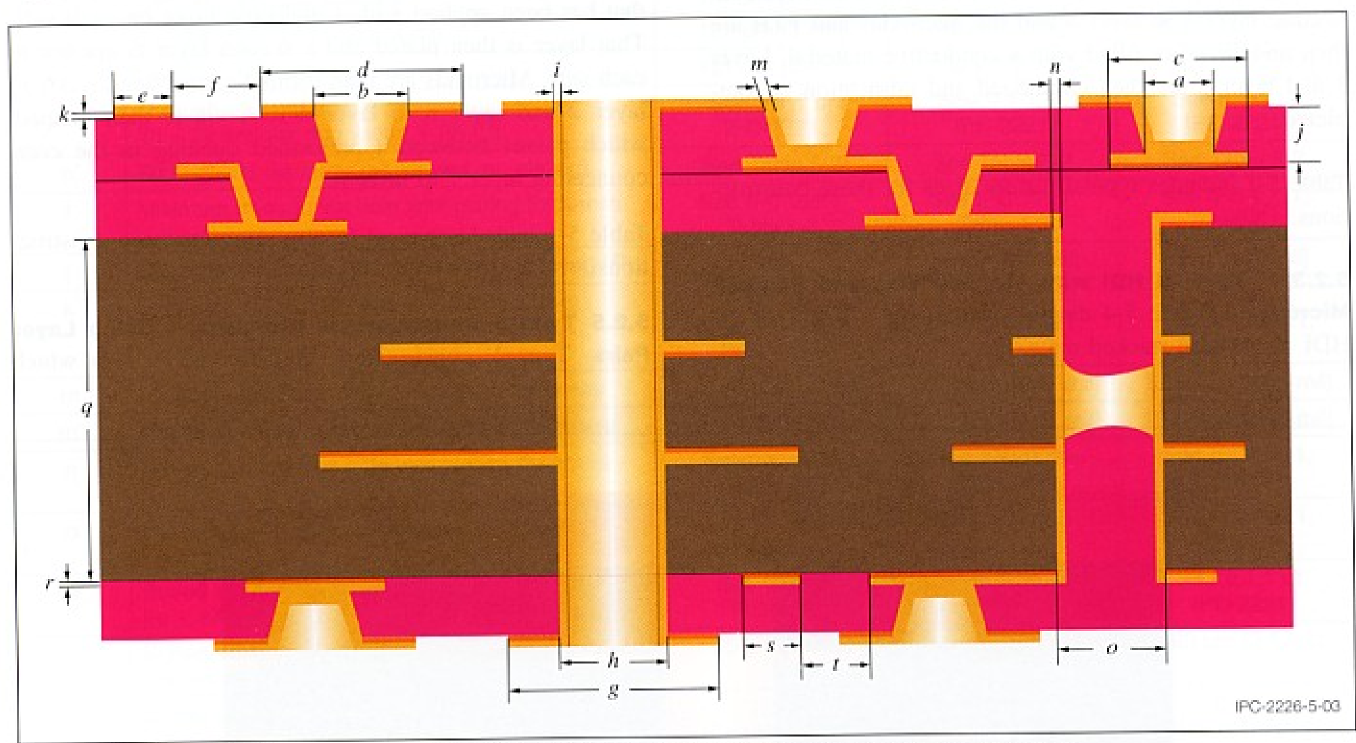


Figure 5-3 Type III HDI Construction (Caution: Unbalanced constructions may result in warp & twist.)

there are both plated microvias and conductive paste interconnections through a co-lamination process. There is essentially no core to this type of construction since all layer pairs have the same characteristics. Type V constructions consist of the fabrication of an even number of layers that are laminated together at the same time the interconnections are made between the odd and even layers. This type of construction is neither build-up nor sequential; it is a single lamination process.

The layer-pair substrates are prepared using conventional processes (i.e., etching, plating and buried vias) and the substrates may be rigid or flexible. The layer pairs are joined together using B-Stage resin systems or some other form of dielectric adhesive into which localized conductive adhesive has been placed. This joining material is used to make the appropriate interconnections. External layers may consist of a single conductive layer, provided its companion layer pair is on the opposite side.

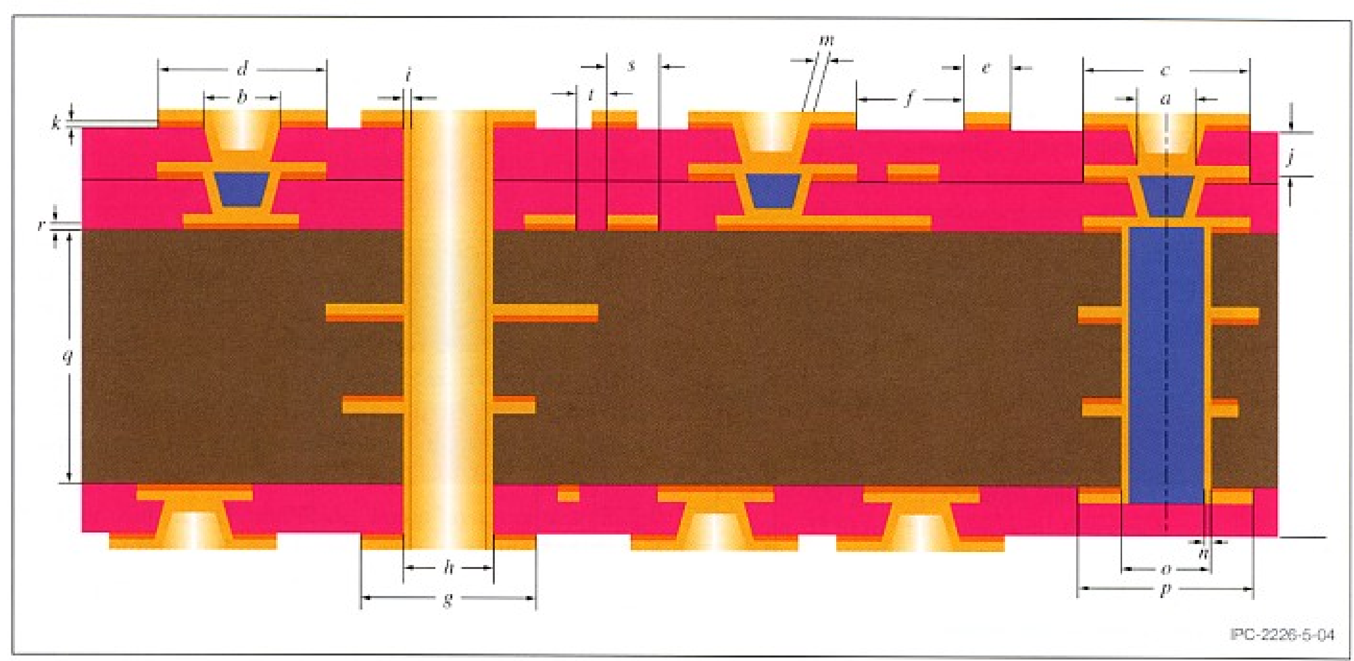


Figure 5-4 Type III HDI Construction with Stacked Microvias (Caution: Unbalanced constructions may result in warp & twist.)

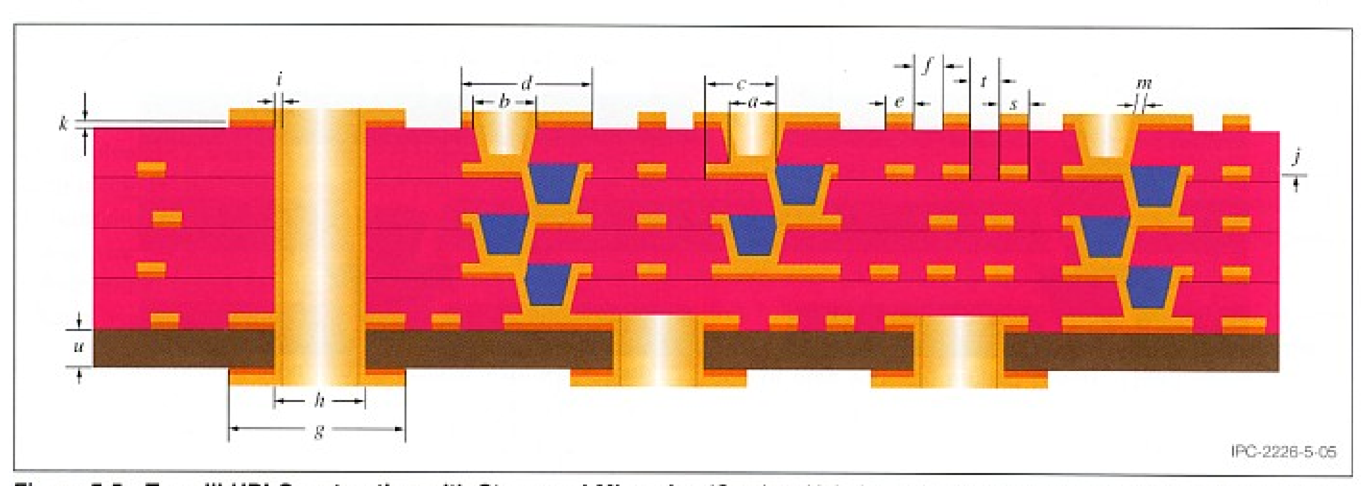


Figure 5-5 Type III HDI Construction with Staggered Microvias (Caution: Unbalanced constructions may result in warp & twist.)

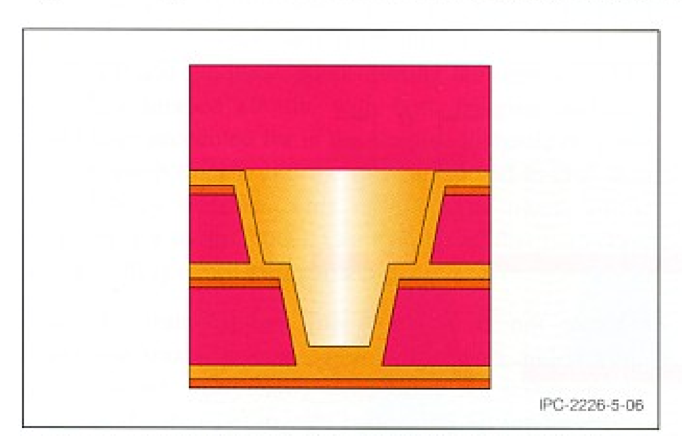


Figure 5-6 Type III HDI with Variable Depth Blind Vias

Figure 5-8 gives an example of a coreless construction using three layer pairs that have been connected in lamination with patterned conductive material and a dielectric adhesive.

Table 5-1 includes typical feature sizes for these constructions.

5.2.6 Type VI Constructions Type VI constructions describe an HDI in which the electrical interconnection and mechanical structure are formed simultaneously. The layers may be formed sequentially or co-laminated and the conductive interconnection may be formed by means other than electroplating (e.g., anisotropic films/pastes, conductive paste, dielectric piercing posts, etc.).

Figure 5-9 gives an example of a Type VI construction that was manufactured using piercing posts. The posts, which are made up of a conductive element, are attached to an unreinforced layer of copper and the bonding process and interconnections are made by adding prepreg and laminating the PCB together in one step.

Table 5-1 includes typical feature sizes for these constructions.

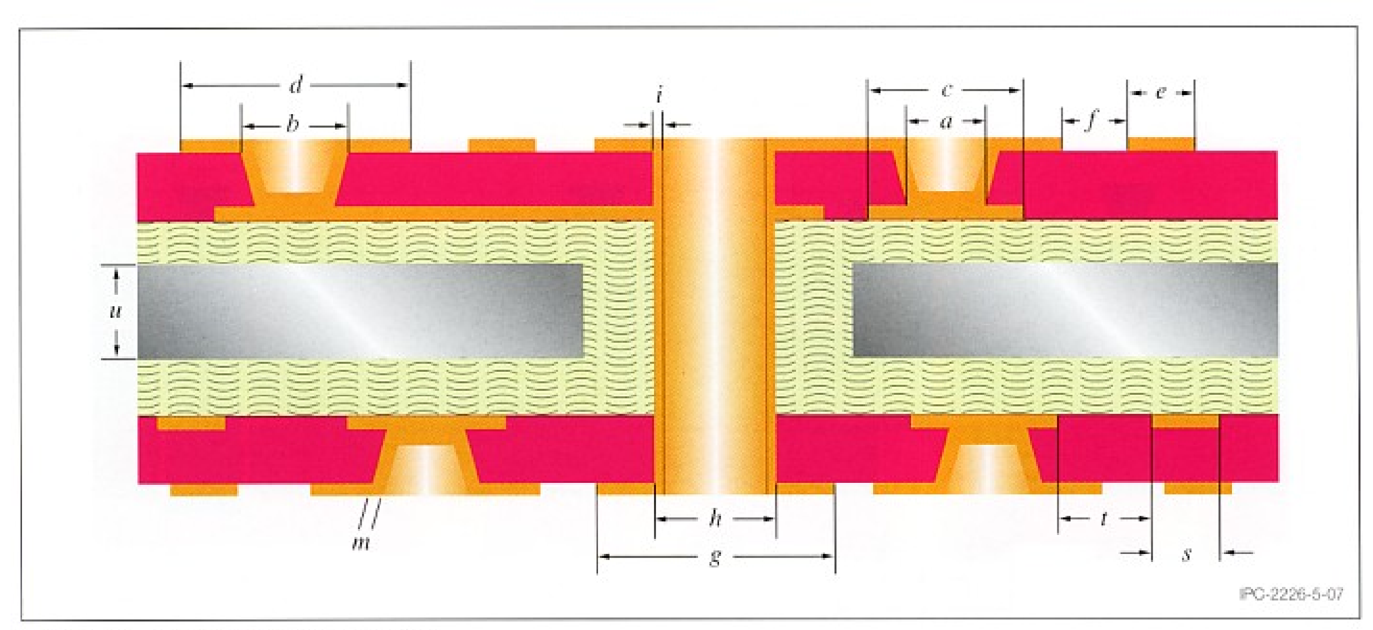


Figure 5-7 Type IV HDI Construction

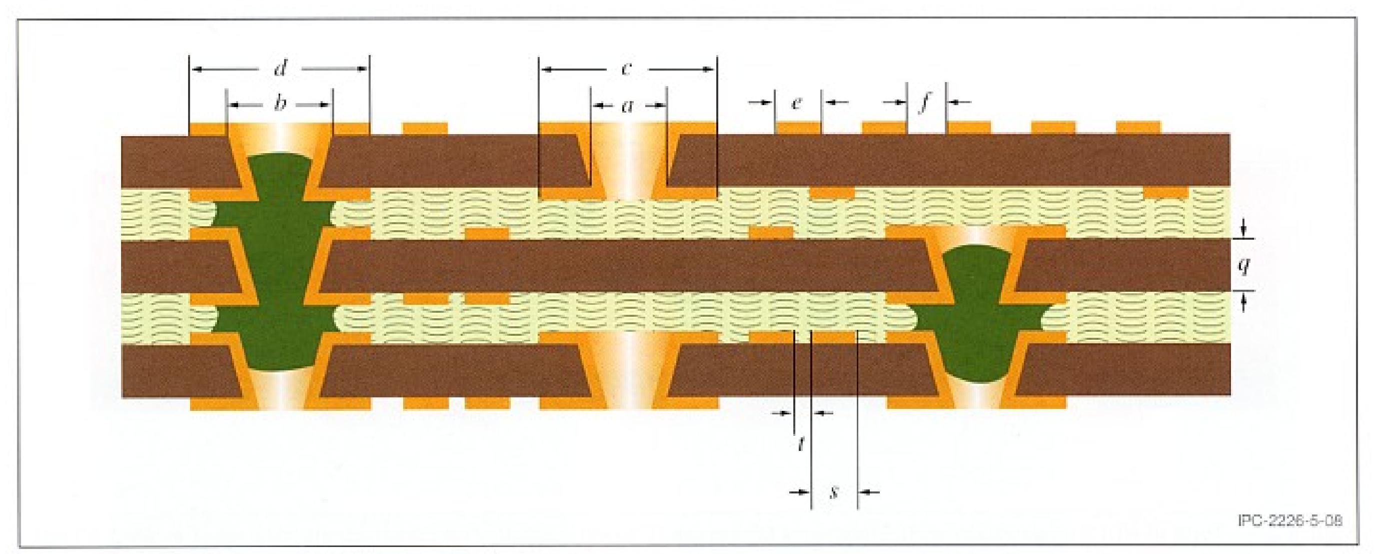


Figure 5-8 Coreless Type V HDI Construction

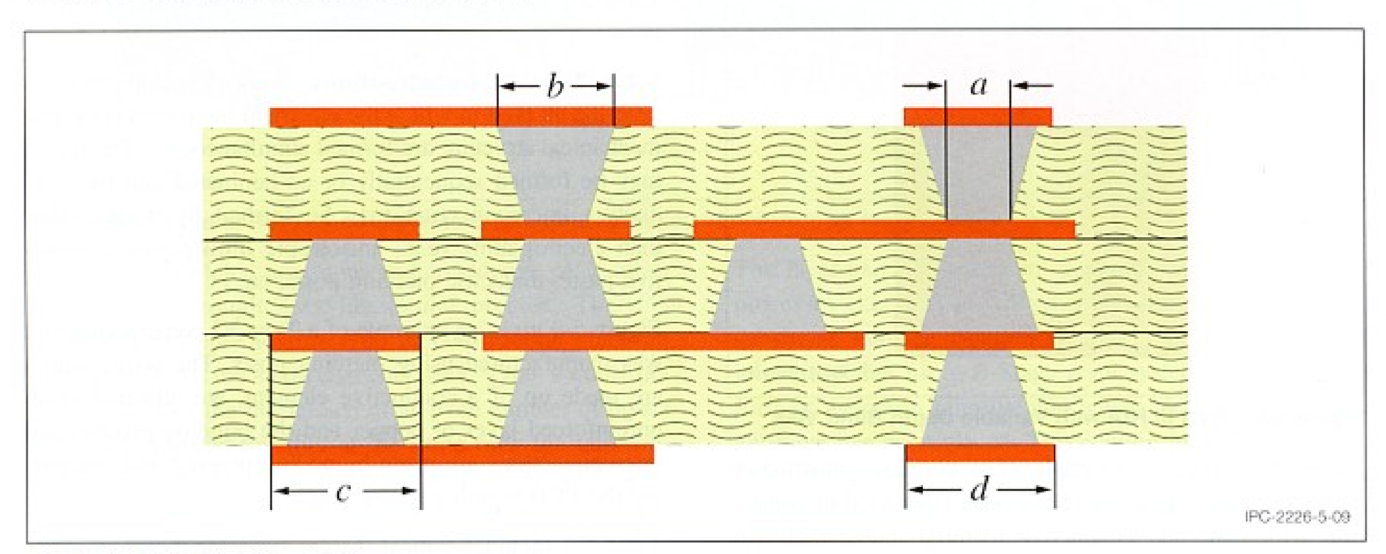


Figure 5-9 Type VI Construction

6 ELECTRICAL PROPERTIES

Electrical modeling analysis and design guidelines relative to chip bumping and flip chip attachment are extremely important considerations. In addition, substrate and package for direct chip attach, electrical models and combined noise analysis of the system must also be addressed.

Bumping technology offers significantly less inductance than wire bonding or TAB interconnects. Although wire bond and TAB chips can be converted to bumped flip chip parts, to take full electrical advantage, chips should be initially designed for the bumping process. This allows optimization of internal chip wiring, circuit placement and bump locations that match the pattern on the HDI substrate.

Whether using a common solder bump layout or designing a new footprint, the chip power, ground, signal and clock pinout must coincide with the substrate pad designations. This is especially true when existing substrates are utilized. Also the location and proximity of sensitive signals must be accommodated. Because bump pitch affects coupling noise, separation and isolation of sensitive signals must be considered in the chip footprint and substrate land pattern design.

6.1 Equivalent Circuitry Figure 6-1 depicts the physical bump electrical path for a peripheral pad chip redistributed for bumping technology. The electrical path consists of a wiring via from the peripheral pad to the Final Metal (redistribution trace), the final metal trace to the pad, the terminal via to the bump.

The substrate metallization and associated wiring are part of the substrate electrical path. The bump electrical equivalent circuitry can be derived as shown in Figure 6-2 for first order approximation.

The wiring via and final metal (trace and pad) are modeled separately. Final metal consists of multiple sections (1...n). The bump and the passivation opening are represented by equivalent lumped circuits with both fringing and area capacitance accounted for in the circuits. It should be noted that the bump-to-chip and the final metal pad-to-chip area capacitances overlap. This coincidence needs to be accounted for in the model. One way to do this is to combine the effect of the two capacitors.

Generally, transmission line modeling is not required unless rise times become significantly short and/or chip-traces become significantly long. Since the bump is relatively short compared to wire bonds or TAB interconnects, lumped element analysis can be used because distributed effects are minimal under most conditions.

6.2 Final Metal Traces The final metal power ground, clock and signal traces are a concern for any chip design but especially for bump redistribution design. Metal thickness has a major impact on final metal resistance (Rfm). Note that metal thickness is limited by the wafer process capability for traces on flip chips.

In the following example, typical dimensions are used to illustrate variations in final metal resistance. For this example the final metal is doped aluminum with the following parameters:

Surface Resistivity (Rs)
= 0.037 ohm/square area (1.0 µm [39.4 µin] thick)
= 0.028 ohm/square area (1.5 µm [59.1 µin] thick)
= 0.018 ohm/square area (2.0 µm [78.7 µin] thick)
Signal Trace = 30 µm [1,181 µin]
Power Trace = 60 µm [2,362 µin]
Trace = 700 µm [27,559 µin] (minimum)
= 3350 µm [131,890 µin] (average)
= 6000 µm [236,221 µin] (maximum)
Trace = 1 µm [39.4 µin], 1.5 µm [59.1 µin] and 2 µm [78.7 µin]

The largest final metal trace resistance (length = 6000 µm [236,221 µin] and width = 30 µm [1,181 µin]) can be calculated from Ohm's law:

R_{FM} = (R_S * Length) / Width = (0.037 Ω * 6000 µm [236,221 µin]) / (30 µm [1.18 mil]) = 7.4 Ω

Using the value from above, Table 6-1 and Table 6-2 provide a quantitative view of how final metal resistance varies according to thickness and length for signal and power traces.

6.2.1 Inductance and Capacitance Calculation of final metal trace inductance and capacitance requires determination of both self and mutual effects. These effects will be unique for each chip design. The orientation of the final metal trace to underlying inter-layer metal and ground planes will determine self and mutual capacitance.

Inductance (L_{FM}) is also influenced by orientation with respect to underlying metal and other Final Metal traces. Direction of current flow in these metal structures must be known to determine mutual inductance. The appropriate current return path is needed to determine self inductance.

Final metal trace capacitance (C_{FM}) consists of self and fringing capacitance. A first order approximation of final metal total capacitance is shown below:

$$C_{FM} = (C_A x L x W) + (C_F x L) \times 2$$

Where:
C_A = Area Capacitance (F/m^2)
C_F = Mutual capacitance (F/m)
L = Trace (m)
W = Trace (m)

For accurate modeling, coupling between final metal traces and underlying traces should be modeled using 2D/3D CAE programs.

Pad

Tract

ILM = Inter-Layer Metal

ILD = Inter-Layer Dielectric

Final Metal

Wiring Via

ILD ILM Silicon

Passivation

Pad Peripheral

Metals Pad Limiting

Terminal Via

Metallization

Substrate

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Figure 6-1 Bump Electrical Path (Redistributed Chip)

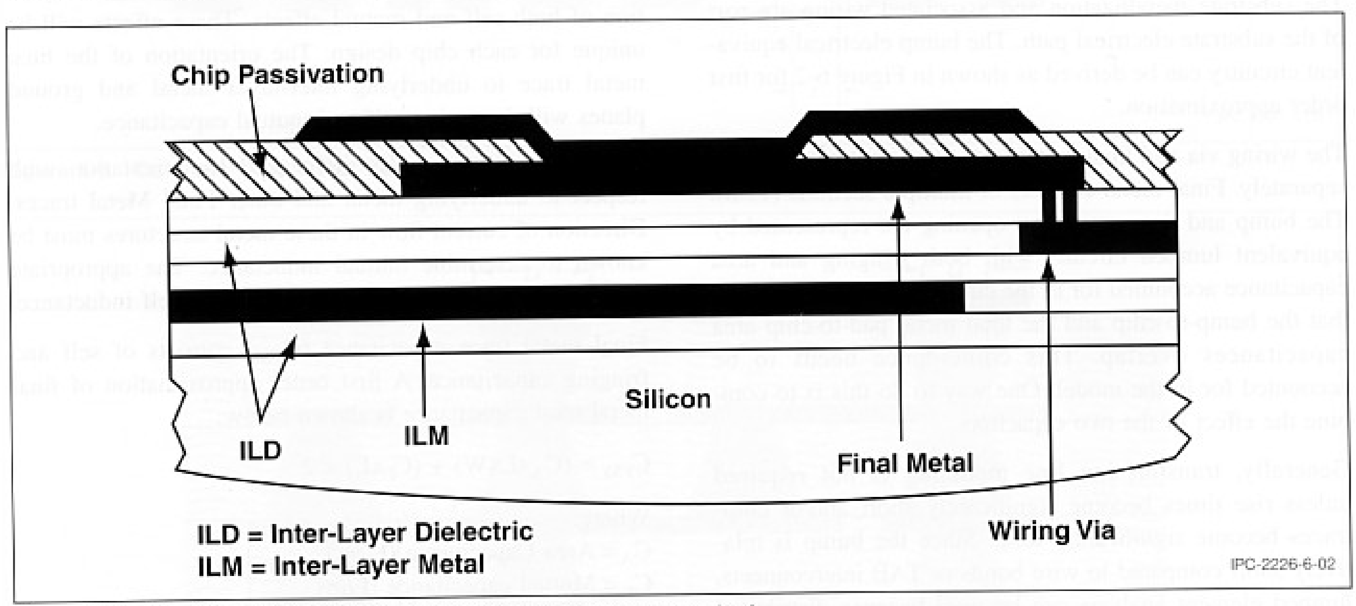


Figure 6-2 Final Metal Trace and Underlying Traces (Cross Section)

Table 6-1 Final Metal Signal Trace (30 µm [1,181 µin]) Resistances (example)

Final Metal Trace	Final Metal Signal Trace Resistance (Ω)		
	1.0 µm [39.4 µin]	1.5 µm [59.1 µin]	2.0 µm [78.7 µin]
700 µm [27,559 µin]	0.9 [35.43 µin]	0.6 [23.62 µin]	0.4 [15.7 µin]
3350 µm [131,890 µin]	4.0 [157.5 µin]	3.1 [122.0 µin]	2.1 [82.6 µin]
6000 µm [236,221 µin]	7.4 [291.3 µin]	5.6 [220.5 µin]	3.7 [145.7 µin]

Table 6-2 Final Metal Power Trace (60 µm [0.00236 in]) Resistances (example)

Final Metal Trace	Final Metal Power Trace Resistance (Ω)		
	1.0 µm [39.4 µin]	1.5 µm [59.1 µin]	2.0 µm [78.7 µin]
700 µm [27,559 µin]	0.4 [15.7 µin]	0.3 [11.81 µin]	0.2 [7.87 µin]
3350 µm [131,890 µin]	2.1 [82.6 µin]	1.6 [62.99 µin]	1.0 [39.4 µin]
6000 µm [236,221 µin]	3.7 [145.7 µin]	2.8 [110.2 µin]	1.8 [70.87 µin]

6.2.2 High Frequency Performance Because the chip active surface is face down or near the active substrate, special consideration in trace routing on the chip, interposer and substrate must be given for flip chips and grid arrays. Changing signal levels on either the chip or the substrate traces close to the chip are coupled.

This coupling creates cross-talk, noises, EMF, interference, etc., in the chip or substrate. Controlling the distance, the dielectric between the chip and substrate traces and characteristic impedance, helps reduce the coupling.

7 THERMAL MANAGEMENT

Thermal aspects of bump packages provide front and/or backside thermal paths. Bump technology offers an added dimension of thermal management. Depending on the application, the designer has the option of selecting the thermal path. This concept differs depending on whether one is designing an HDI product as part of a component board or as part of a product board. In the component board analysis, the main thermal mechanism comes from the die. Usually this is the back of the bare die and the thermal management is made through that plane. As an example, if the component is a wire-bonded die attach, then the component board must have a copper surface intended to remove or transfer heat from the bottom of the die. If the component board encompasses a flip chip design, the thermal management must be accomplished from the top of the die and therefore a special heatsink is usually developed which helps create the thermal path. The additional heatsink is in all probability the most efficient form of thermal management, though some cooling can be affected through the ball topology of the flip chip device.

The component board thermal path is made through internal copper layers and vias that make their connection to the ball that serves as the transfer medium to the thermal plane. These balls, normally attached to thermal vias, do not necessarily perform an electronic function and are primarily intended to establish the thermal path from the bottom of the die through the component board onto the ball and finally to the cooler surface of the product board. In this regard, the product board must have a strategy to prevent the heat from building up at the surface of the board where the ball is attached. Additional thermal vias thus serve as a mechanism for transferring heat from the thermal ball of the component board into the product board structure, usually connecting to a thermal plane. The major differential between the product board and the component board relative to thermal management is that the thermal plane of the product board can also perform an electronic function, i.e., ground or voltage plane.

The degree of consideration given to thermal design is dependent upon three factors:

1. The amount of energy or heat that must be dissipated.
2. The desired operating junction temperature of the bare die.
3. The ambient temperature of the surrounding environment.

Conduction, convection and radiation are the models for which power can be dissipated. For bump interconnects, conduction is the primary heat dissipation mode with convection and radiation being smaller contributors.

The thermal management concerns for components mounted on HDI substrates need to be addressed separately from concerns for the core substrate. Nevertheless, the transfer technology is usually related to the metallic surfaces contained within the product board. The heat transfer from any source is accomplished through conduction from the component to the metal surfaces on any product board, regardless of whether the product is an HDI or conventional multilayer product. It should be understood that the thicker the copper thermal path, the easier the transfer of heat to a cooler plane. Figure 7-1 shows the path through two HDI surface layers (Layers 1 and 2) and it is not until the heat reaches the through hole where any effective cooling can take place. It is for this reason that many components have several thermal transfer paths to optimize the transfer mechanism through the thinner copper layers of the HDI board.

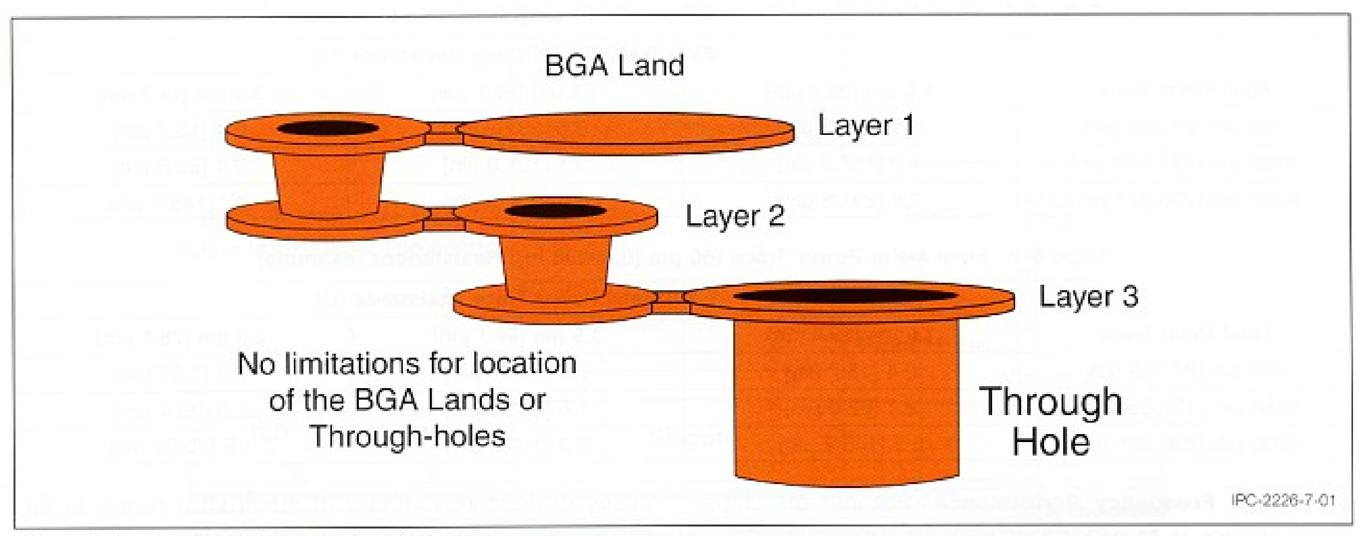


Figure 7-1 HDI Thermal Path Relationships

The forthcoming IPC-2152 will deal with the cooling effect of ground and voltage planes within a multilayer board structure. The focus of that standard will concentrate on the cooling effect that the planes have on those conductors that generate a great deal of heat due to the amperage they carry. IPC-2152 will define the conditions separating a high thermal conductor from its associated cooling plane. The transfer of heat is through the dielectric which is not the most conducive for the heat transferring conditions. It has been established that the resin and glass structure of the dielectric play a role in the amount of heat that can be transferred between a conductor and a cooling plane, thus both material and dielectric separation should be a part of that analysis as will be defined in the IPC-2152. As these same principles apply when trying to move heat from the surface, one normally attempts to use vias as the transfer mechanism to the plane, rather than a conductor.

There are many similar conditions between the electrical characteristics of a product board and the resistance to the flow of electrons in a conductor. It is understood that copper used in product boards has the least resistance and thus one could think of heat transfer as taking on the same properties, migrating along a path that has the least resistance to the thermal transfer from a heated device or surface to that which is cooler. Figure 7-2 shows how thermal and electrical analysis are analogous to one another.

7.1 Thermal Management Concerns for Bump Interconnects on HDI The bump thermal interconnect can be modeled as two cylinders between the chip power source and the HDI substrate (see Figure 7-3). Cylinder I represents the innerlayer materials on the chip. Cylinder II represents the pad limiting metals and the bump size. The heat source is the device in the chip.

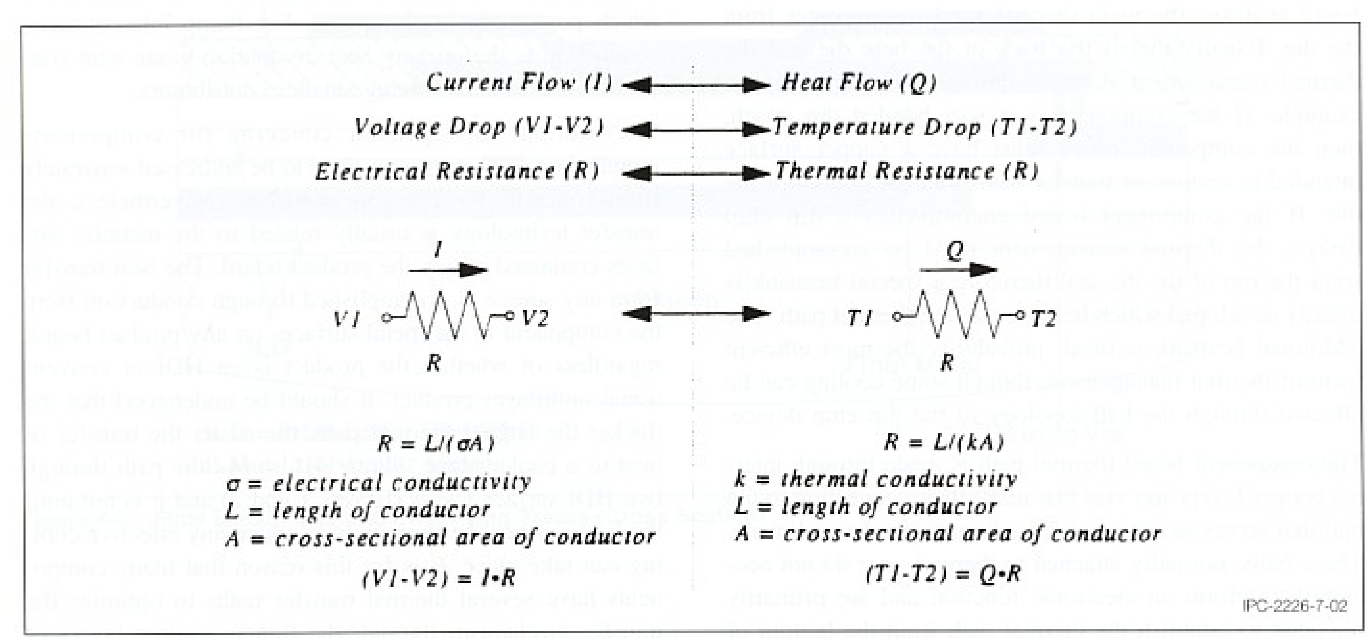


Figure 7-2 Thermal Management of Chip Scale and Flip Chip Parts Mounted on HDI

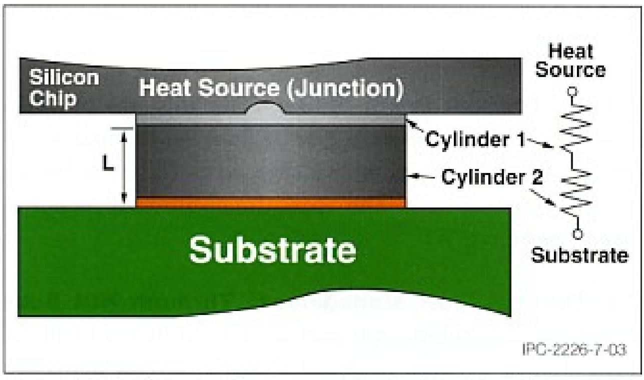


Figure 7-3 Bump Interconnect Equivalent Model

Because there are three bump interconnect diameter options, cylinder sizes vary accordingly. Assuming that Cylinder I is SiO 2 (k = 1.01 W/mK) and Cylinder II is tin/lead (3/97) solder (k = 36 W/mK) then the approximate interconnect thermal resistance can be calculated for each option (see Table 7-1).

It should be noted that Cylinder I thermal resistance varies according to the number and specifically, the thickness (L) of innerlayers on the chip. As the main contributor to thermal resistance, it should be modeled accurately. Furthermore, interface and bulk resistances have been combined to simplify calculations and illustrations.

Bump interconnect thermal resistance for a typical single, double and triple layer metal device are shown in Table 7-2. It should be noted that these values are based on 150 µm [5,906 µin] bump on silicon where SiO 2 inter-layer dielectric is modeled.

7.1.1 Junction to Case Thermal Models Packaging options can range from hermetic, metallized ceramic modules to printed circuit boards and HDI for direct chip or chip scale packaging for highly specialized thermal conduction packages. A bare die mounted on a substrate has a relatively simplistic thermal model. It consists of the heat path through the ball from the chip to the metal on the substrate. Other materials such as chip underfill, used to improve reliability by enhancing the CTE relationship between the die and the substrate, can also alter heat dissipation. Supplemental package features like incorporating a heat sink into the package design change the major transfer path of those parts that follow that packaging concept. Thermal paste can be added to enhance the thermal performance to facilitate heat transfer from the die to the heatsink. All these components influence the junction to case thermal models.

Table 7-2 Typical Bump (150 µm) [5,906 µin] Thermal Resistance Multilayer Metal Chips

	Single Layer	Double Layer	Triple Layer
Maximum (°C/W)	550	750	950
Nominal (°C/W)	450	650	850
Minimum (°C/W)	350	550	750

7.1.1.1 Wire Bond Thermal Model The wire bond thermal model consists of the substrate directly transferring most of the heat from the die as shown in Figure 7-4. The die is directly attached to a platform either with conductive epoxy or thermal paste. There is no heat transfer from the wires that interconnect the chip bonding sites to the lands on the component board substrate. All heat transfer in the wire bond thermal model is accomplished from the platform through thermal vias, either into a cooling plane in the component board or to solder balls located at the base of the component. These balls then become the method for transferring heat from a wire-bonded BGA. To enhance the thermal properties, most manufacturers fill the thermal vias with a thermal conductive epoxy. The approximate thermal model is shown in Figure 7-5.

7.1.1.2 Flip Chip Thermal Model The flip chip thermal model has some different characteristics for heat transfer essentially based on the fact that it is important for the flip chip to match the CTE of the mounting substrate. Because of these requirements, flip chip concepts require a substrate that has a CTE similar to the silicon die. A ceramic substrate fits that objective and thus provides some additional benefits in thermal management in that the ceramic substrate has excellent heat transfer properties. Figure 7-6 shows the characteristics of a bare die in a flip chip position on a ceramic substrate. The thermal path comes from

Table 7-1 Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip)

Interconnect Option	Diameter (µm) [µin]	Cylinder I			Cylinder II			Total R (°C/W)
		L (µm) [µin]	A(Π²) (nm²)	R (°C/W)	L (µm) [µin]	A(Π²) (nm²)	R (°C/W)	
Option A	150 µm [5,906 µin]	10 µm [394 µin]	18	550	75 µm [2,953 µin]	18	116	666
Option B	150 µm [5,906 µin]	10 µm [394 µin]	13	762	63 µm [2,480 in]	13	135	897
Option C	150 µm [5,906 µin]	10 µm [394 µin]	8	1238	50 µm [1,969 µin]	8	174	1412
Option D (DCA)	150 µm [5,906 µin]	10 µm [394 µin]	18	550	≥75 µm [2,953 µin]	18	≥116	≥666

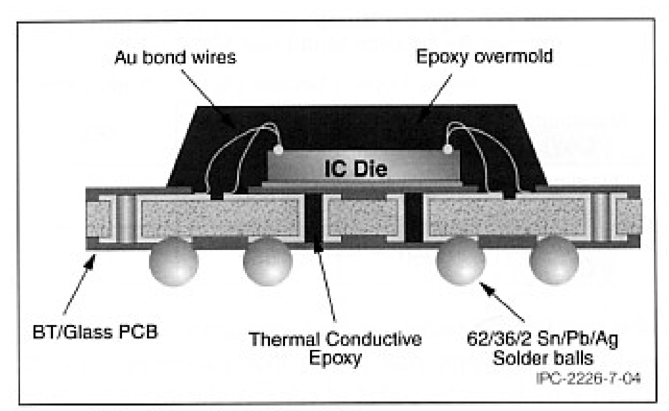


Figure 7-4 Wire Bond Example

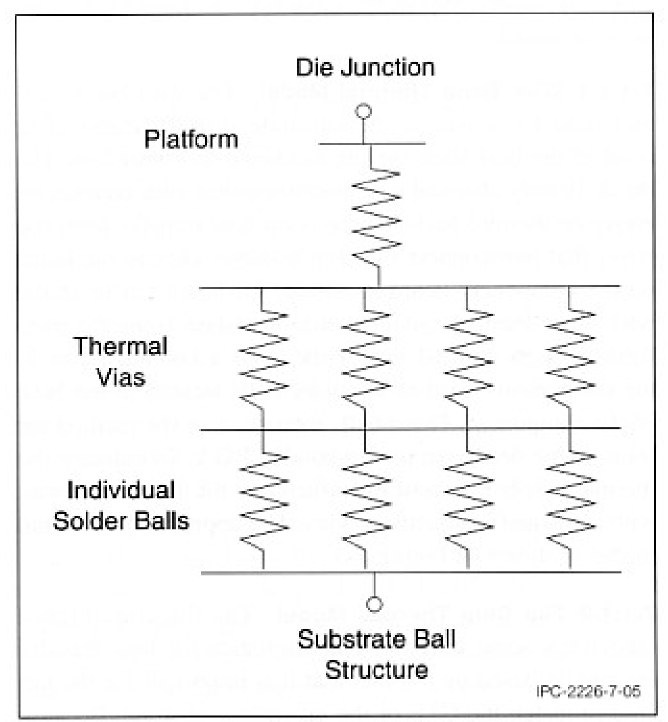


Figure 7-5 Approximate Thermal Model for Wire Bond

the back of the die, through the silicon, to the balls on the chip. Those balls then transfer the heat to the conductive surfaces on the ceramic substrate which becomes the major cooling function. The balls used for mounting the ceramic substrate may be eutectic or a high lead (5Sn95Pb) ball. These balls transfer the heat from the ceramic component substrate to the next level of interconnect. Figure 7-7 shows the approximate thermal model.

7.1.1.3 Flip Chip with Underfill Underfill is used to enhance reliability for flip chip applications where the die is mounted to an organic substrate or product board. The intent of the underfill is to create a mechanical bond between the organic substrate (component or product board) and the silicon of the die. Underfill is dispensed between the chip and substrate surrounding the bumps as shown in Figure 7-8. It must be properly cured in order to achieve the desired CTE effect between the die and the substrate. Because the underfill completely fills the gap between the chip and substrate, it does change the thermal model. The approximate model is shown in Figure 7-9.

7.1.1.4 Thermal Paste Model The thermal paste is applied to the chip backside to reduce the thermal resistance between the chip, the package lid as shown in Figure 7-10 or the heat sink. The approximate thermal model is shown in Figure 7-11.

7.2 Thermal Flow Management Through HDI Substrate In determining the analysis for the thermal path of any component board or product board, several items are considered as important in the evaluations. The first of these is the length of the heat transfer path. The path usually starts as previously explained with the semiconductor die, continues on through the component and its mounting substrate and eventually winds up in the product board, hopefully in a cooling plane.

It has been explained that the path is a function of the material used and the cross sectional area of the path that transfers the heat. This cross-sectional area relates to the volume as well as to the area, thus for HDI with relatively thin metallic surfaces, an additional resistance must be considered if the path includes the HDI product in getting to the cooler surfaces.

The following general equation can be used to determine the conditions of heat transfer.

Thermal Resistance

$R = L/KA$

Where:
L = length of heat transfer path
K = material thermal conductivity
A = cross sectional area through heat transfer path

An example utilizing this equation is given below.

Let:

$L = 10\ \mu m$
$K = 1.01\ W/m\text{-}K$
$A = \Pi\ D^2/4$ where $D = 150\ \mu m$
$A = 3.14 * (150)^2/4$
$A = 17.6\ E03\ \mu m^2$

$$R = \frac{10\ \mu m}{1.01\ W/m\text{–}K * 17.7E03}\ \frac{1.0\ E06\ \mu m}{1\ m}$$

$W/m\text{-}K \equiv W/m\text{-}C$

$R = 560\ °C/W$

From the analysis it can be seen that thermal vias are normally considered by their total volume contribution to the heat transfer equation. In many instances this is determined as a round cylinder (see Figure 7-12), however cross-sectional area volume can also be identified for a plane that

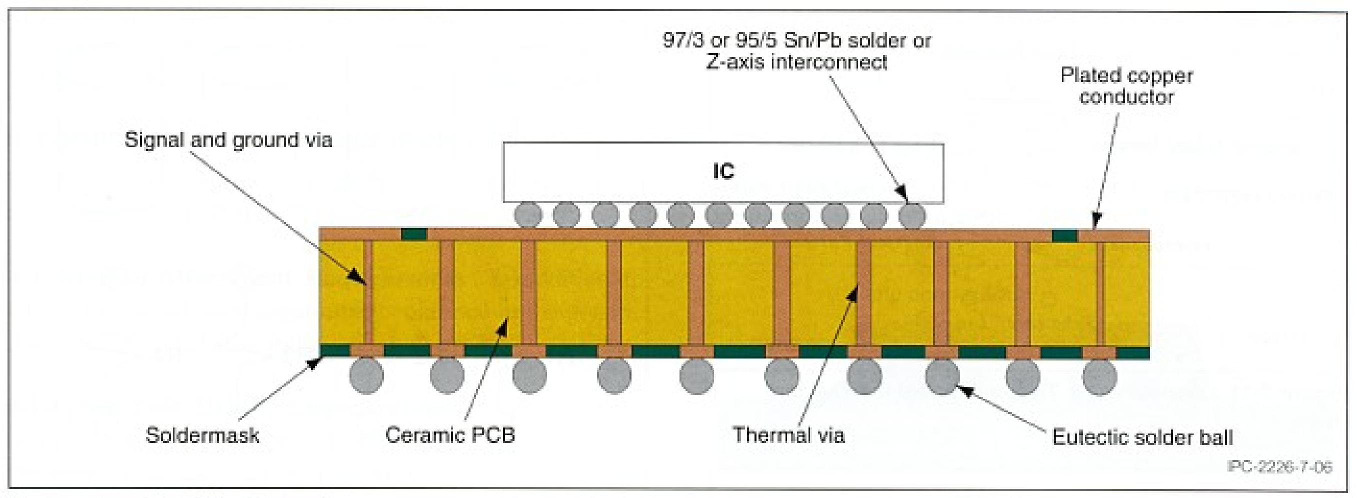


Figure 7-6 Flip Chip Example

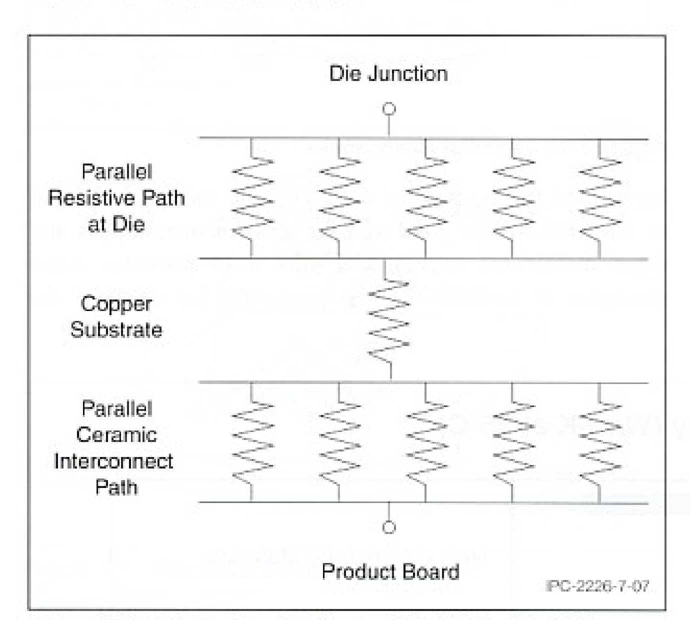


Figure 7-7 Approximate Thermal Model for Flip Chip

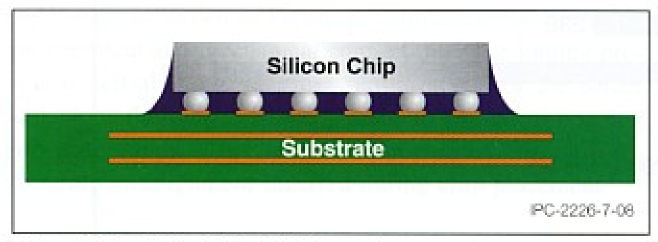


Figure 7-8 Chip Underfill Example

acts as a cooling surface for the HDI product. It should be noted that in determining the characteristics of a plane, one must take into consideration a certain amount of copper that has been removed from the plane to accommodate plated-through holes that do not connect; thus its total contribution is somewhat reduced.

In designing HDI product as shown in this standard, the type most useful for heat transfer is that which contains through vias in the HDI structure. These through vias normally are larger and less resistive and therefore are more

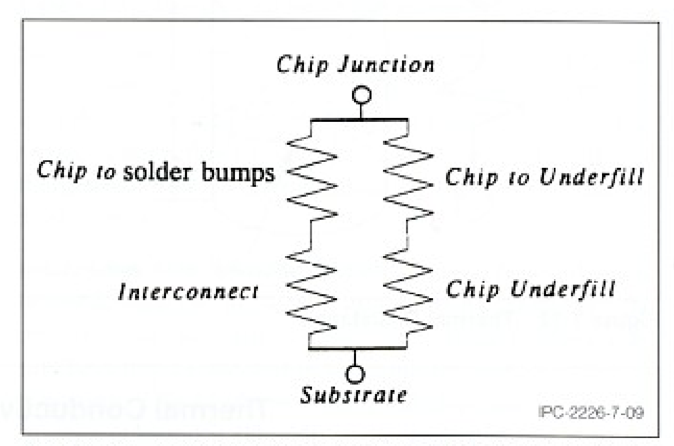


Figure 7-9 Approximate Thermal Model for Chip Underfill

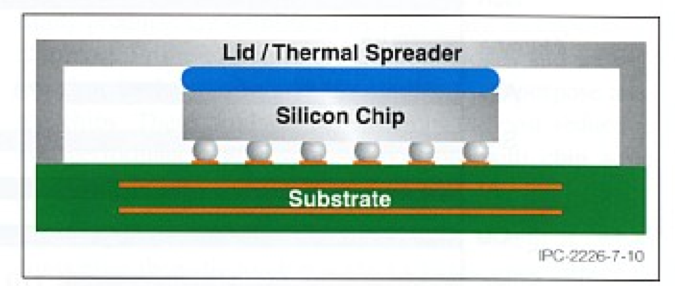


Figure 7-10 Thermal Paste Example

accommodating for heat transfer. A good design is one that takes full advantage of the concept of through hole vias by utilizing them as thermal vias for the purpose of removing heat from the component down to a cooling plane, as opposed to using the HDI conductive pattern as a part of the thermal path.

Whenever multiple thermal vias are used to remove heat, their characteristics **shall** be considered in accordance with Figure 7-13. The illustration shows that the volume of the thermal via is calculated and evaluated in parallel in order to determine the full thermal resistance.

In order to complete the evaluation of the thermal path, one needs to know the thermal conductivity of the material

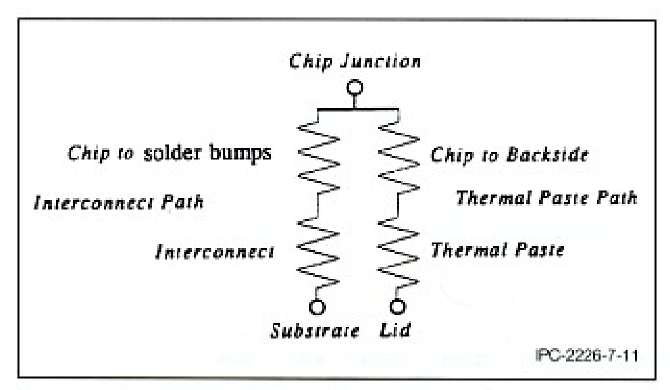


Figure 7-11 Approximate Thermal Model for Thermal Paste

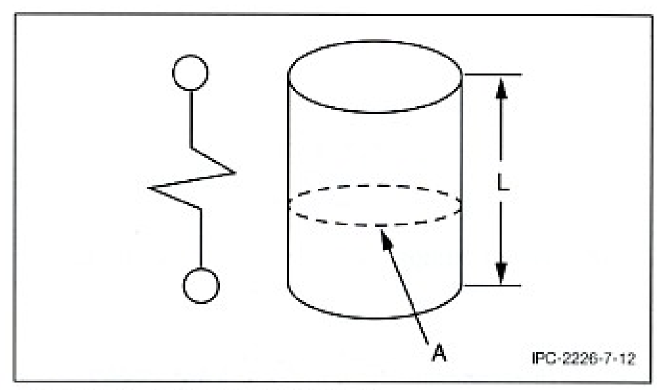


Figure 7-12 Thermal Resistance

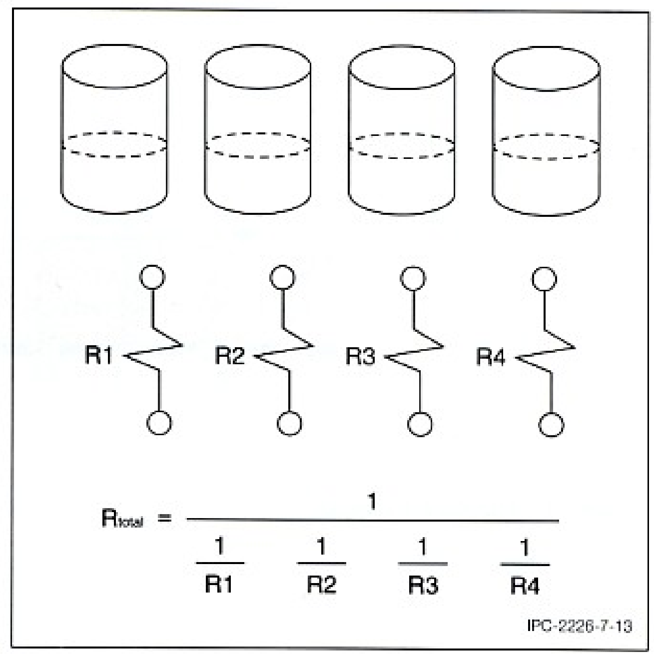


Figure 7-13 Parallel Resistances

being used for the thermal path. Organic substrate material or underfill are not good transfer mechanisms; copper and other metals are excellent. Figure 7-14 provides some examples of metallic thermal properties for some of the

Thermal Conductivity (W/m-K at 25°C)

Material	W/m-K	Group
Beo	250	Hybrid Substrate Materials
Alumina	27	Hybrid Substrate Materials
AlN	170	Hybrid Substrate Materials
SiC	240	
Al	238	
Cu	398	
CuMo	170	
CuW	200	
CuW	180	
Kovar	17	
AlSiC	180	
GaAs	54	IC Materials
Si	151	IC Materials
Polyimide	0.35	Board Laminate Materials
FR-4	0.30	Board Laminate Materials

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Figure 7-14 Metallic Thermal Properties

more popular metals used either in the electronic conductive patterns or as heat spreaders or heat sinks on either the component, the component board or the product board.

8 COMPONENT AND ASSEMBLY ISSUES

Component assembly issues **shall** be in accordance with the generic standard IPC-2221 and as follows:

8.1 General Attachment Requirements In addition to the general attachment requirements outlined in the generic standard IPC-2221, the following **shall** apply:

8.1.1 Flip Chip Design Considerations Flip chip technology is an interconnection technology developed during the 1960s as an alternative to manual wire bonding. In this methodology the chip is attached to circuitry facing the substrate. Solder bumps are deposited onto a wettable chip pad that connects to matching wettable substrate lands as shown in Figure 8-1.

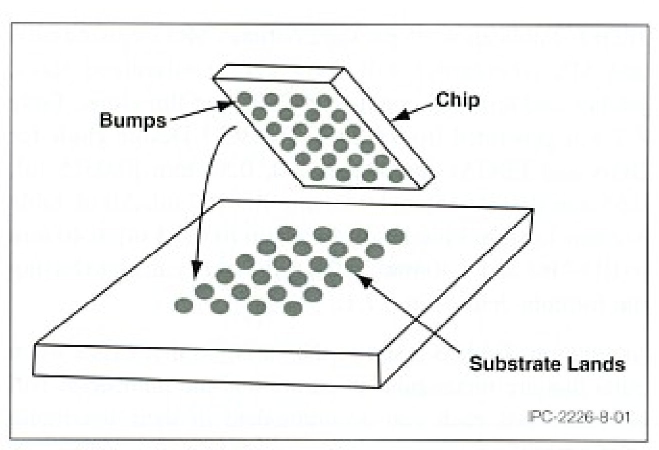


Figure 8-1 Flip Chip Connection

Flipped chips are aligned to corresponding substrate metal patterns. Interconnections are formed by reflowing the solder bumps as shown in Figure 8-2 simultaneously forming the electrical and mechanical connections. The joining process is self-aligning, i.e., the wetting action of the solder will align the chip bumped pattern to the corresponding substrate lands. This action compensates for chip-to-substrate misalignment incurred during chip placement.

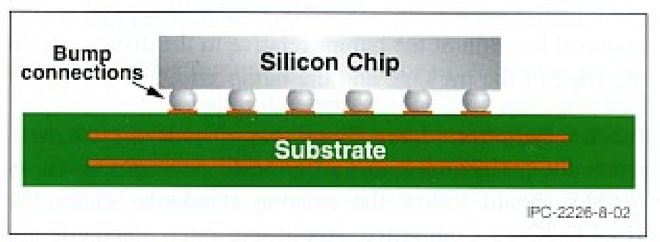


Figure 8-2 Mechanical and Electrical Connections

An added feature of the flip chip process is the potential to rework. Several techniques exist that allow the removal and replacement of chips without scrapping the chip or substrate. Depending on substrate material, rework can be performed numerous times without degrading the quality or reliability provided that the mounting substrate can tolerate the rework temperatures. Injection of chip underfill, as illustrated in Figure 8-3, improves reliability most notably in cases of high mechanical stress. It should be noted that currently any rework must be performed prior to the application of chip underfill.

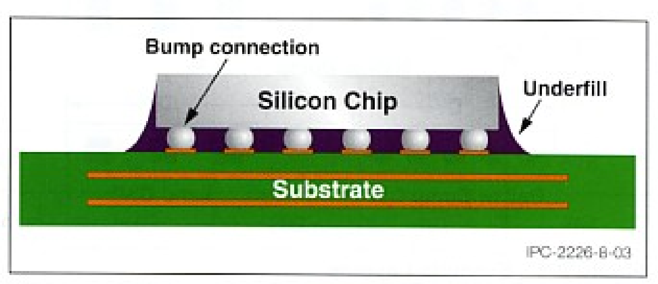


Figure 8-3 Joined Chip and Chip Underfill

An alternate joining technology to reflowable bump flip chip is one that has low melting solder bumps attached directly to a printed board. The bump on the semiconductor die is not reflowed, instead the lower melting solder on the printed board wets the bump on the die to form the interconnect.

8.1.2 Chip Size Standardization Standardizing the size of semiconductor chips may appear to be counter to the objectives of the chip designer and supplier. Many chip suppliers rely on the ability to shrink the size of a chip as it matures. This results in more good chips per wafer. This strategy is sound if the chip is the dominant cost item for the product.

Many products are dominated by packaging, as opposed to chip cost. Prime examples are discrete diodes and transistors, low lead count logic devices and general purpose analog chips. These products benefit from the cost reduction and performance improvements possible with chip scale packaging (CSP).

Chip suppliers and their customers will benefit if, when converting their die to chip scale packages, they adhere to area size standards. Accepting chip size standards will reduce the need for many different tape stocks for the tape and reel packaging of these devices. Standards will also allow users multiple sources for the same device.

The dimensions of flip chip dice are determined mainly by the design and wafer processing and are therefore difficult to impose standards. However, the standardization of the interconnection pattern will reduce the costs for Known Good Die (KGD), die test, burn-in and handling. Recommended footprints would use standard pitches and an appropriate grid for the interconnect attributes (see Figure 8-4).

There are various pitches that impact the characteristics of the balls/bumps/lands and the number of each of the conditions that exist. In order to determine the relationships

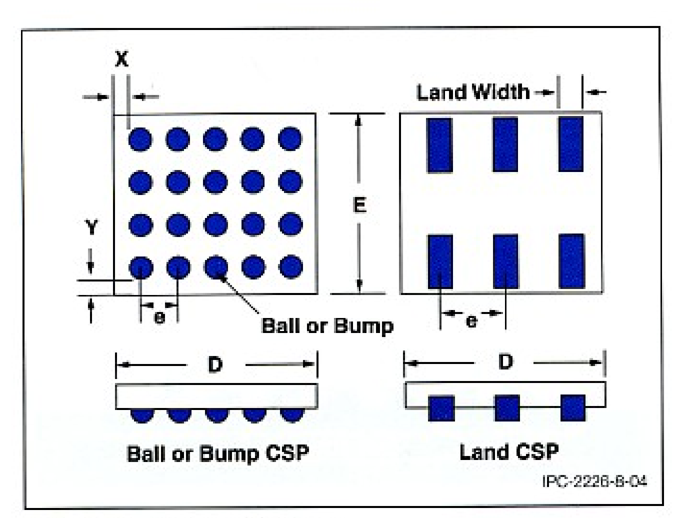


Figure 8-4 Example Layouts

between number of balls and chip size, the characteristics of the different pitches are noted in Table 8-1.

JEDEC Design Standard 95-1, Section 5 specifies the relationship between the size of the die or CSP and the maximum number of ball or bumps that a configuration can accommodate. The standard identifies an equation for the length (D) and width (E) configuration as well as the tolerances for the location of the ball or bumps, the allowance to die or CSP edge conditions from the ball or bump (X and Y, Figure 8-4) and tolerance for the size die.

The equation states that the maximum ball or bump count (MD or ME) for either the D or E Chip or CSP body direction can be determined using the following:

$$MD = \frac{[(D-aaa)-(b_{max}+eee)]-(2x)}{e}+1$$

truncated to the next integer

or

$$ME = \frac{[(E-aaa)-(b_{max}+eee)]-(2y)}{e}+1$$

truncated to the next integer

Where:

D = the length of the die or CSP

E = the width of the die or CSP

aaa = the variation from nominal D or E (usually 0.15 mm [0.00591 in])

b_{max} = maximum ball or column diameter (can also be applied to land width where lands are on the edge of a die or CSP).

eee = location tolerance variation from true position (usually 0.50 DTP)

X = distance of maximum ball/bump/land from chip or CSP edge (D side), usually 0.13 mm [0.00512 in]

Y = distance of maximum ball/bump/land from chip or CSP edge (E side), usually 0.13 mm [0.00512 in]

8.1.2.1 I/O Capability Table 8-2 and Table 8-3 show the characteristics of die or CSP that are square and rectangular in size. It should be noted that for nonsquare die or CSP, the examples shown are based on a package ratio of approximately 2:3. It should also be understood that the intent of the table is to provide information on the I/O capability for various chip and CSP sizes using the previously defined equations and the maximum ball/column diameter shown in Table 8-2.

The column headings of Tables 8-3 and 8-4 highlight the drivers for chips and CSP related to pitch distances. The examples provide expectations for I/O for the fixed sizes indicated using pitch variations from 1.00 mm [0.0394 in] to 0.30 mm [0.0118 in].

JEDEC Publication 95 package outlines MO (registrations) and MS (standards) will show the standardized sizes, pitches and terminal counts for CSPs and flip chips. Table 8-2 was generated from JEDEC Pub 95-1 Design guide for BGA and FBGAs for pitches 1.0, 0.80 mm [0.0315 in], 0.65 mm [0.0256 in] and 0.50 mm [0.0197 in]. All of Table 8-2 and Table 8-3 pitches of 0.75 mm [0.0295 in], 0.40 mm [0.0157 in] and 0.30 mm [0.0118 in] were calculated using the formula defined in 8.2.1.

In addition, Table 8-3 shows the variation that exists when parts that are rectangular in nature and the number of ball positions that each can accommodate in their maximum relationships.

8.1.3 Bump Site Standards The chip scale bump grid array packages give chip designers significant freedom to chose the bump location and the signal type transmitted on the bump. Chip suppliers should observe standards for grid pitch, bump size and bump location.

Optical assemblers will use placement machines that will place the package based on the edge dimensions. This is because the machine can't see the bump locations. The placement accuracy and assembly yield will depend on the assumed location of the bumps relative to the distance from the edge of the package and the bump grid.

8.1.3.1 Peripheral Lead Standards The lead pitch standards for peripheral leaded chip scale packages, such as MSMT should follow the existing standards set by the JEDEC JC-11 Committee. Applicable pitch standards are

Table 8-1 Pitch Dimensions

Standard pitch			Fine pitch				Very fine pitch		
1.50 mm [0.0591 in]	1.27 mm [0.05 in]	1.0 mm [0.0394 in]	0.80 mm [0.0315 in]	0.75 mm [0.0295 in]	0.65 mm [0.0256 in]	0.50 mm [0.0197 in]	0.40 mm [0.0157 in]	0.30 mm [0.0118 in]	0.25 mm [0.00984 in]

Table 8-2 Examples of Fixed Square Body Size Showing Maximum I/O Capability

Size Identifier	Size Limitations mm, [in]	Potential I/Os Related to Pitch						
		1.0 mm [0.0394 in]	0.8 mm [0.0315 in]	0.75 mm [0.0295 in]	0.65 mm [0.0256 in]	0.50 mm [0.0197 in]	0.40 mm [0.0157 in]	0.30 mm [0.0118 in]
S1	4x4 [0.16x0.16]	9	16	25	25	49	81	121
S2	5x5 [0.20x0.20]	16	25	36	49	81	121	196
S3	6x6 [0.24x0.24]	25	49	64	64	121	196	289
S4	7x7 [0.28x0.28]	36	64	81	100	169	256	441
S5	8x8 [0.32x0.32]	49	81	100	121	225	361	576
S6	9x9 [0.35x0.35]	64	100	144	169	289	441	784
S7	10x10 [0.394x0.394]	81	144	169	196	361	476	961
S8	11x11 [0.433x0.433]	100	169	196	256	441	676	1156
S9	12x12 [0.472x0.472]	121	186	256	289	529	841	1444
S10	13x13 [0.512x0.512]	144	225	289	361	625	961	1681
S11	14x14 [0.551x0.551]	169	289	324	400	729	1156	1936
S12	15x15 [0.591x0.591]	196	324	400	484	841	1296	2304
S13	16x16 [0.630x0.630]	225	361	441	529	961	1521	2601
S14	17x17 [0.669x0.669]	256	400	484	625	1089	1681	2916
S15	18x18 [0.709x0.709]	289	484	576	729	1225	1936	3364
S16	19x19 [0.748x0.748]	324	529	625	784	1369	2116	3721
S17	20x20 [0.787x0.787]	361	576	676	900	1521	2401	4096
S18	21x21 [0.827x0.827]	400	625	784	961	1681	2601	4624

0.2 mm [0.00787 in], 0.3 mm [0.0118 in], 0.4 mm [0.0157 in], 0.5 mm [0.0197 in], 0.63 mm [0.0248 in] and 0.65 mm [0.0256 in]. Refer to JEDEC publication 95 for detailed dimensions.

8.1.4 Bump Options

8.1.4.1 Solder Bump The solder bump forms the electrical and mechanical bridge between the chip and next level assembly. It absorbs the stress between the chip and next level of assembly caused by variations in their relative thermal expansion rates.

The solder composition of the flip chip bumps varies according to required mechanical and thermal properties.

Electrodeposition offers a wider range of SnPb composition than evaporation and thus offers greater control over mechanical and thermal properties. Electrodeposition also produces smaller diameter bumps and is more difficult to control uniformity.

A variety of solder paste compositions can be screen printed.

Common bump diameters and minimum pitches are shown in Table 8-4. Minimum pitch requirements are based on radial distances (center to center) between bumps. Bump diameters are measured at the widest point of the ball.

Common bump compositions include:

- 50 InPb
- 63 SnPb
- 90 PbSn
- 95 PbSn
- 97 PbSn

Table 8-3 Example of Fixed Rectangular Body Size

Size Identifier	Size Limitations mm [in]	Potential I/Os Related to Pitch						
		1.0 mm [0.0394 in]	0.8 mm [0.0315 in]	0.75 mm [0.0295 in]	0.65 mm [0.0256 in]	0.50 mm [0.0197 in]	0.40 mm [0.0157 in]	0.30 mm [0.0118 in]
R1	4x3 [0.16x0.12]	9	12	20	20	35	54	88
R2	5x3 [0.20x0.12]	12	15	24	28	45	66	112
R3	6x4 [0.24x0.16]	15	28	40	40	77	126	187
R4	7x5 [0.28x0.20]	24	40	54	70	117	176	294
R5	8x6 [0.32x0.24]	35	63	80	88	165	266	408
R6	9x6 [0.35x0.24]	40	70	96	104	187	294	476
R7	10x7 [0.394x0.28]	54	96	117	140	247	384	651
R8	11x7 [0.433x0.28]	60	104	126	160	273	416	816
R9	12x8 [0.472x0.32]	77	126	160	187	345	551	912
R10	13x9 [0.512x0.35]	96	150	204	247	425	651	1148
R11	14x9 0.551x0.35]	104	170	216	260	459	714	1232
R12	15x10 [0.501x0.394]	126	216	260	308	551	864	1488
R13	16x11 [0.630x0.433]	150	247	294	368	651	1014	1734
R14	17x11 [0.669x0.433]	160	260	308	400	693	1066	1836
R15	18x12 [0.709x0.709]	187	308	384	459	805	1276	2204
R16	19x13 [0.748x0.512]	216	345	425	532	925	1426	2501
R17	20x13 [0.787x0.512]	228	360	442	570	975	1519	2624
R18	21x14 [0.827x0.551]	260	425	504	837	1107	1734	2992

Table 8-4 Bump Diameter and Minimum Pitch Options

Deposition Types	Diameter (µm) [µin]	Minimum Pitch (µm) [µin]
(A) Evaporation or Electro-deposition	150 [5,906] 125 [4,921] 100 [3,937]	300/350 [11,810/13,780] 250 [9,843] 225 [8,858]
(B) Screen Printing	200 [7,874] 150 [5,906] 125 [4,921]	375 [1,476] 250* [9,843] 200* [7,874]

*Peripheral only.

Today, for flip chip applications, minimum pitch requirements are larger to account for printed board wiring capabilities.

An example of typical DCA bump design is shown in Figure 8-5.

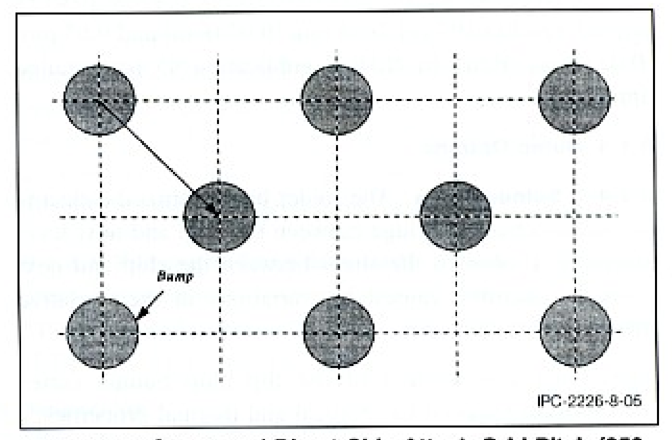


Figure 8-5 Suggested Direct Chip Attach Grid Pitch (250 µm [9,843 µin] Grid; 150 µm [5,906 µin] Bumps)

8.2 Chip Scale Design Considerations Flip chip bumping processes have lead to the development of concepts identified as chip scale interconnection. Chip scale (size) packages are extensions of that concept that have been enhanced to provide more robust attachment technology. Although initially thought of as only array type packages, the concept for CSP has grown to cover various constructions of single die or multiple dies in a package configuration. Figure 8-6 shows three variations of package constructions. In each instance the package is slightly larger than the bare die, thus these parts are sometimes known as chip size packages.

Having die encapsulated in this more robust configuration enhances the assembly process. Chip scale packages parallel standard surface mount packages in form factor, being found in both peripherally leaded and area array formats. As with their larger counterparts, chip scale packages are designed to facilitate test and burn-in of the semiconductor before committing them to the assembly process, thus effectively providing an answer to the current problem of known good die (KGD).

Chip scale packaging (CSP) has emerged as a viable semiconductor packaging technology that seeks to bridge the gap between flip chips and conventional surface mount packages.

The technology has developed in response to some of the limitations of flip chip technology and to address the concerns and perceived risks associated with handling and assembling bare die while still maintaining most of the volumetric packaging and performance advantages that flip chip technology offers.

The common advantage of these differing approaches is the ability to offer packaged chips that will facilitate movement toward smaller, lighter, high performance systems at lower cost, using the current SMT assembly infrastructure.

The need for smaller devices, the developments in flip chip bumping processes and advancements in the packaging of microwave devices have lead to the development of chip scale package concepts. CSPs are extensions to the flip chip concept as the packaging of the chip provides robust handling and attachment without the need for additional materials, such as underfill epoxies.

Chip scale packages are available in two basic configurations;

1. Chip Scale Area Array Packages (FBGA and FLGA).
2. Chip Scale Peripheral Leaded Packages (TSOJ and SOC).
3. Chip Scale Peripheral Land Packages (SON and QFN).

Chip scale packages are attached to the HDI using the basic fine pitch surface mount technology assembly process.

The fine pitch process starts by stenciling a thin layer of fine particle solder paste onto the PCB land areas. Next, the bumps, balls or leads of the chip scale and other SMT packages are placed in contact with the solder paste. The assembly is heated in a controlled oven to a temperature above the melting temperature of the solder. The assembly is cleaned, if required. As with flip chip, an underfill epoxy may be injected under and around the chip scale devices to enhance their solder joint reliability, however, like conventional SMT, certain chip scale packages do not require the underfill epoxy. After curing the underfill epoxy, the assembly is tested.

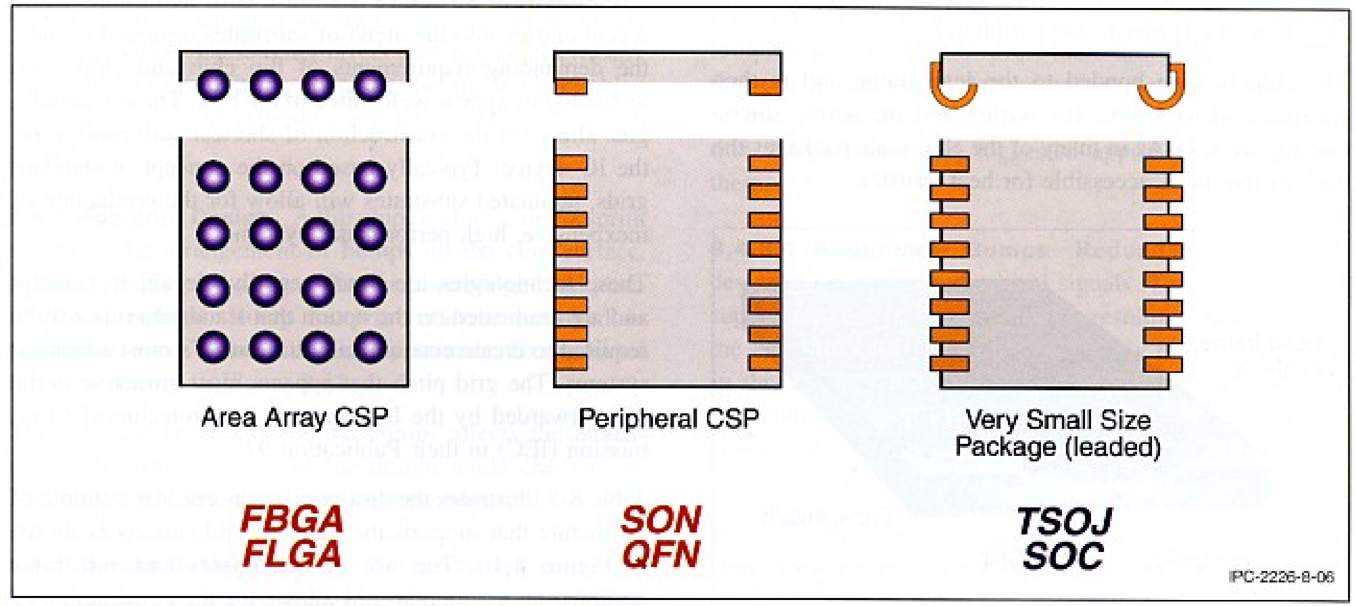


Figure 8-6 Type of CSP

8.2.1 Chip Scale Area Arrays (FBGA and FLGA) Chip scale Grid Arrays are produced by a few different fabrication methods. The CSP-A configurations developed to date include:

- Micro BGAs
- Mini BGAs
- SLICC
- Other chip scale packages

Each has its unique method of manufacture, however, most of the devices contain an interconnection method for the chip on the top side in an array format similar to flip chip.

In the case of μBGA and SLICC a flexible or rigid interposer serves at the redistribution dielectric. In the case of mini BGA and CSPs the dielectric is a polyimide which is deposited on the active part of the chip.

8.2.2 Peripheral Leaded Chip Scale Packages (TSOJ and SOC) Peripheral leaded chip scale packages are those that make use of or replace the existing bonding pads on the semi-conductor chip. TAB is one form of peripheral package and qualifies as a chip scale package if the TAB area is within the area defined for chip scale packages. (More information is available on TAB in the document SMC-TR-001).

Beam lead technology is another chip scale peripheral approach that is still used for microwave devices. New ideas for chip scale packages have developed. One of these is the Micro SMT or MSMT package. This package consists of metallized silicon or GaAs posts and metal beams. The chip, the posts and the beams are encapsulated in an epoxy or similar compound.

A second CSP-S is the system that uses a lead frame. The lead frame provides the redistribution of the chip bonding sites from the corner to the peripheral.

The chip is wire bonded to the lead frame and is then encapsulated to protect the wiring and the active silicon (see Figure 8-7). As in many of the chip scale packages the back of the die is accessible for heat transfer.

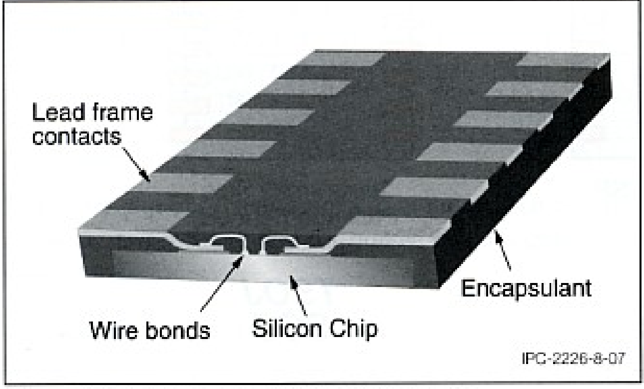


Figure 8-7 Chip Scale Peripheral Package

The major difference between the two peripheral packaging systems is that the MSMT is accomplished at the wafer level.

8.3 Printed Board Land Pattern Design The Printed Board Land Pattern for flip chips and grid arrays is simply a circle of coated copper whose diameter is the same as the bump's circle. The coating on the copper is one of the common solderability preservatives, such as solder, gold flash or an organic solderability protector (OSP).

For MSMT packages, the land pattern may be a solder mask defined opening over the conductive area. A top and cross sectional view of the printed board land pattern is shown in Figure 8-8 and Figure 8-9.

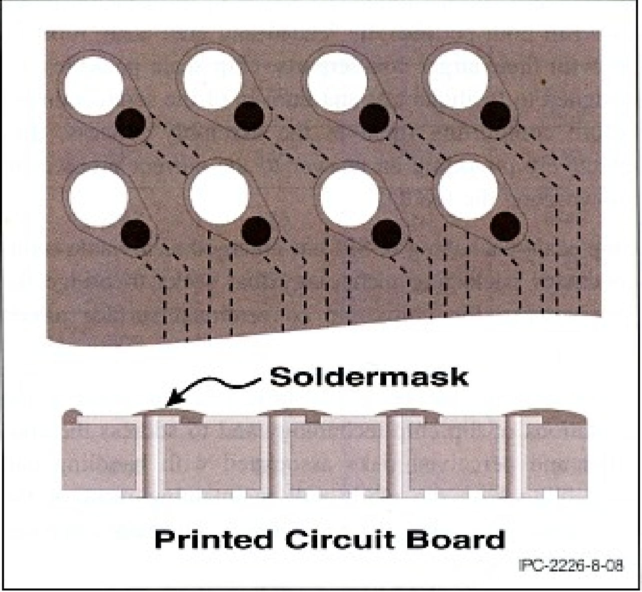


Figure 8-8 Printed Board Flip Chip or Grid Array Land Patterns

8.4 Substrate Structure Standard Grid Evolution More recent entries into the arena of substrates designed to meet the demanding requirements of flip chip and chip scale technologies appear well suited to the task. These technologies allow for the construction of shortest path routing for the IC device. Typically based on the concept of standard grids, laminated substrates will allow for the production of inexpensive, high performance systems.

These technologies are fundamentally elegant in concept and are predicated on the notion that standard grids will be required to create economically tomorrow's most advanced systems. The grid pitch that appears most attractive is the one forwarded by the International Electrotechnical Commission (IEC) in their Publication 97.

Table 8-5 illustrates the design rule concept. An example of a structure that supports the standard grid concept is shown in Figure 8-10. The use of interposers and substrates designed on a common grid allows for the construction of substrates that can offer "Manhattan routing" of signals.

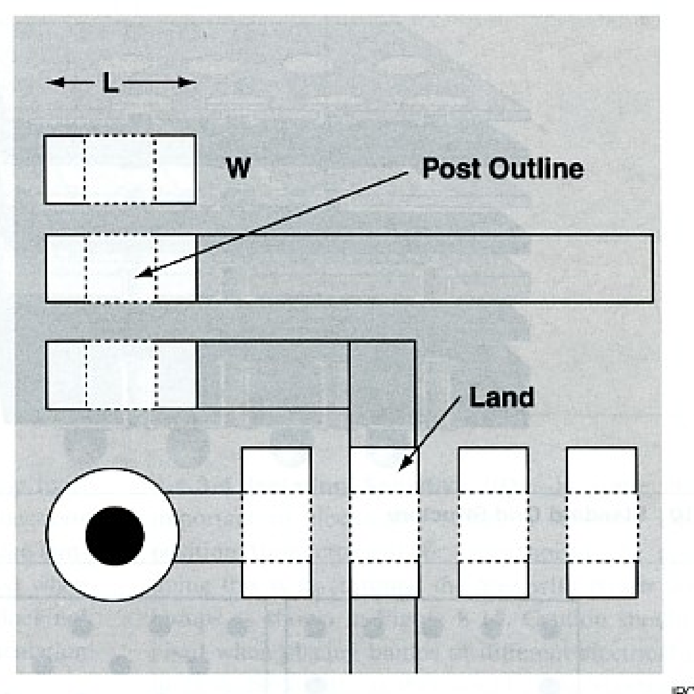


Figure 8-9 MSMT Land Drawing and Dimensions

Table 8-5 Chip Edge Seal Dimensions (Typical)

Description	Dimension	Width
Chip Passivation Edge Seal	A	A.R
Polyimide Edge Seal	B	7 µm [276 µin]

This eliminates the need for redistribution wiring, which normally consumes large amounts of valuable board real estate while limiting higher performance opportunities.

In the illustrated format the interposer joins the inner layers and interconnects them in a single step process. Because the inner layers are thin, the plated through-holes have very small aspect ratios for plating and are relatively easy to produce. These inner layers can then be electrically tested before committing them to the finally assembled laminate stack, thus providing greater assurance of a high yield.

8.4.1 Footprint Design A flip chip or chip scale footprint design is the arrangement of bumps on the chip surface. When laying out the array of bumps, forethought and planning are required. Bump footprints can be arranged in peripheral, array or interstitial array formats. Examples of these are shown in Figure 8-11.

The size and population of the bumps affects the attachment reliability. The use of the design guide checklist in J-STD-012 will minimize reliability problems.

8.4.2 Design Guide Checklist Various design guidelines are applicable in the development of the chip, the CSP or the attachment process. The guidelines in some instances relate directly to the chip manufacturing conditions. In other instances they also apply to chip scale I/Os. In any event, the guidelines are for very specific reasons and designers should consider the following issues:

8.4.3 Footprint Population The number of bumps needed varies with electrical, thermal and mechanical requirements. Besides electrical connections, bumps may be included for heat dissipation, mechanical support (outriggers, chip orientation or future design migration).

Each application has its own unique characteristics. This makes it impossible to establish a general methodology for footprint population; however, there are various strategies that can be employed depending on the application. The following are some examples of several footprints population design issues and suggested approaches for solving them.

8.4.3.1 Redundant Bumps Redundant bumps are designed for power and critical signals. The chip area will support a larger footprint but the resulting distance from the neutral point (DNP) may negatively impact reliability. In this approach the outermost rows of bumps join chips and endure the most stress. As the DNP increases, the stress in the outer rows increases.

By placing redundant bumps in the outer rows and critical bumps in the inner rows, if bumps in the outer rows fail, chip functionality will not be compromised. Include a sufficient number of redundant bumps to allow for potential loss. Figure 8-12 shows how this might be accomplished.

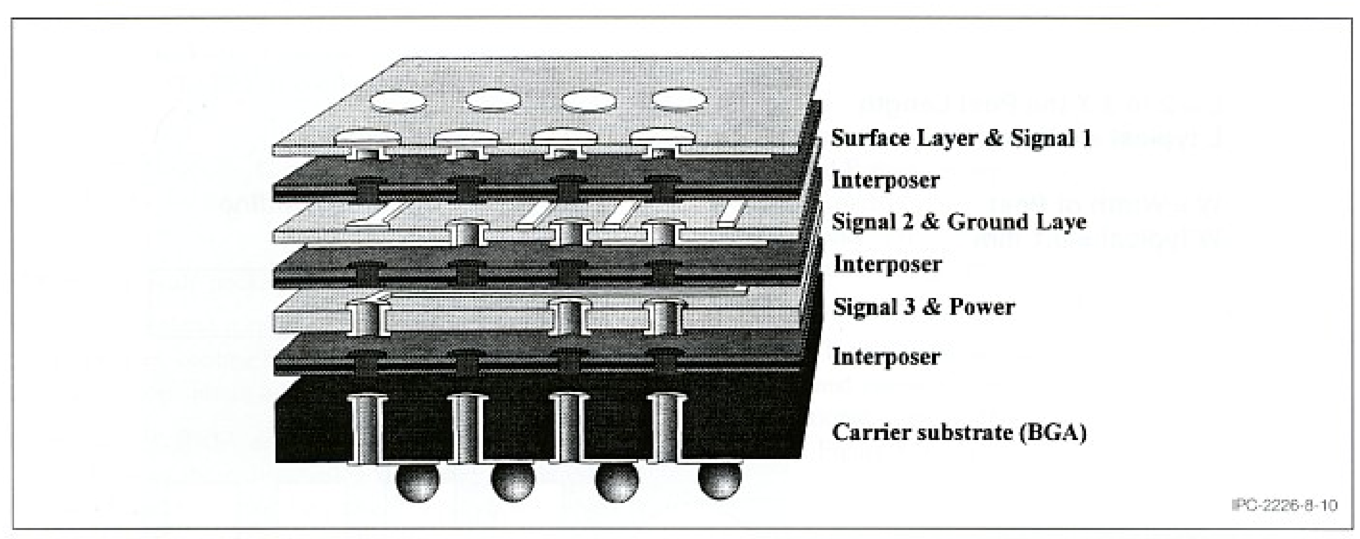


Figure 8-10 Standard Grid Structure

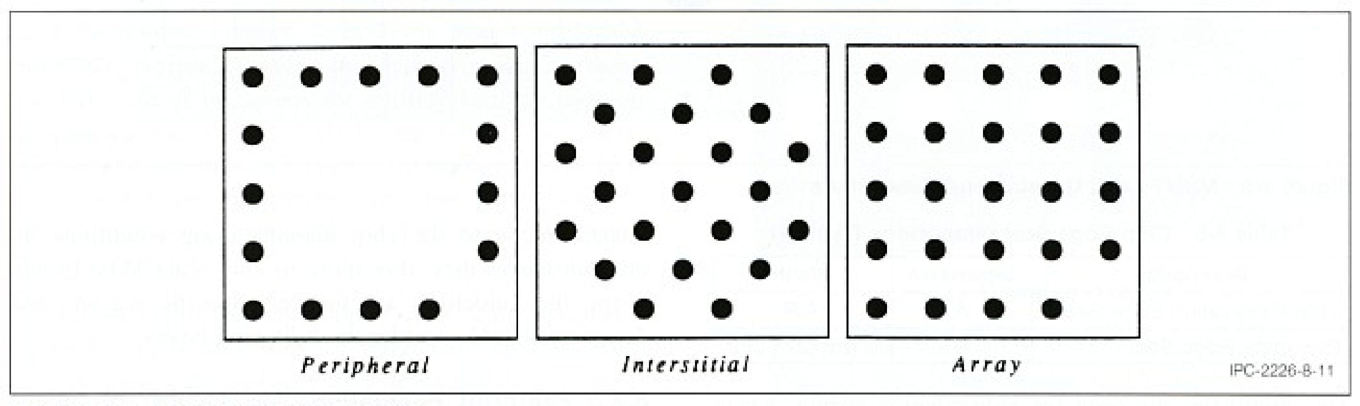


Figure 8-11 Bump Footprint Planning

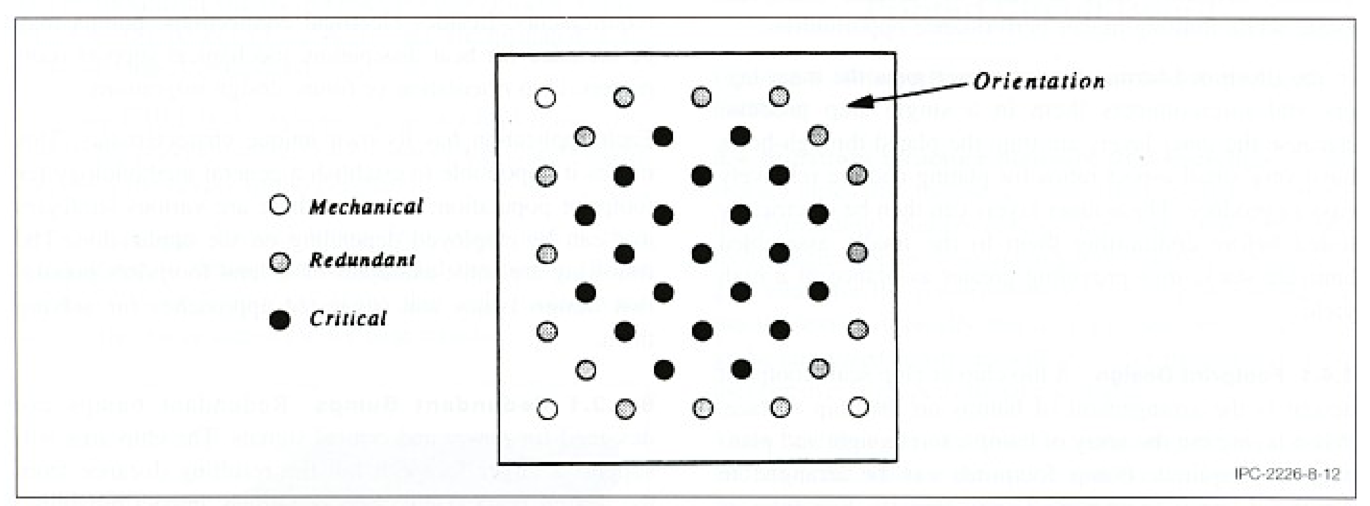


Figure 8-12 Redundant Footprint

An alternative and supplemental solution would be to use chip underfill after the chip is attached to a substrate. This might be necessary if the DNP is sufficiently large. This does not involve additional wafer level processing.

8.4.3.2 Chips That Will Incur Design Shrinks Designing a footprint for chips that incur design shrinks requires additional considerations. The approach for this chip design is to locate the critical bumps in the chip's interior. Use outer rows for redundant and mechanical bumps. When the shrink occurs, the outer, less essential rows will be lost, but the critical bumps will not be affected. As the chip shrinks so does the DNP -making the loss of redundant and mechanical bumps less of an issue. This is illustrated in Figure 8-13.

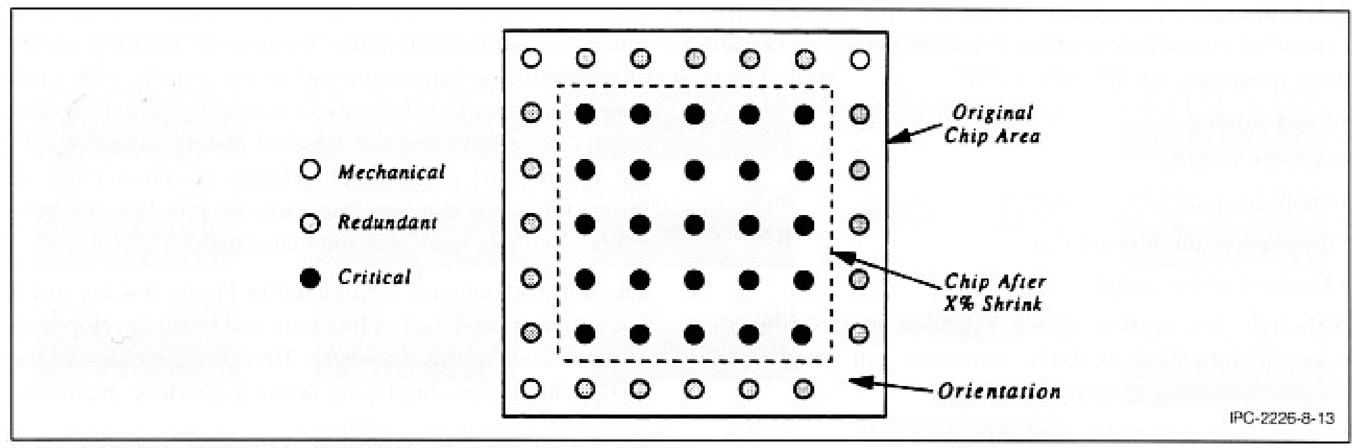


Figure 8-13 Design Shrink Footprint

It should be noted that with this approach, the bump footprint does not affect the package, as the critical connections do not change. Redundant connections to the package simply become open pins. Caution should be exercised when the chip area shrinks so that the bump footprint does not shrink. In addition, provision must be made for orientation and alignment of the shrunk die.

8.4.3.3 I/O Drivers on the Periphery Some chip designs require that the I/O drivers are on the periphery with other circuits internal to the chip. Redundant connections for power and signals are desired.

When using the approach that positions I/O drivers on the chip periphery, shorter interconnection lengths are always desirable in order to minimize parasitic effects. Bumps should be located as close to the pertinent circuitry as possible.

Figure 8-14 shows redundant power and ground bumps that are located above the internal circuitry to minimize distribution lengths. Input bumps are placed near the input circuitry and output bumps are placed near the output drivers.

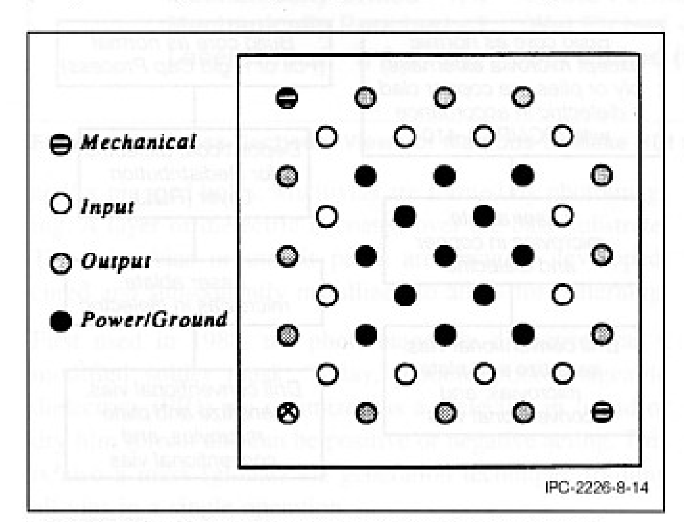


Figure 8-14 Signal and Power Distribution Position

8.4.3.4 Isolating Sensitive I/Os In some chips, it is important to electrically isolate a sensitive input/output position from crosstalk or other noise. The approach to doing this is to surround the area with power and ground bumps as shown in Figure 8-15. Caution should be exercised when placing bumps of different electrical potentials in close proximity, as they could cause shorting problems with dense wafer probes. Bump pitch should be maximized to minimize this hazard.

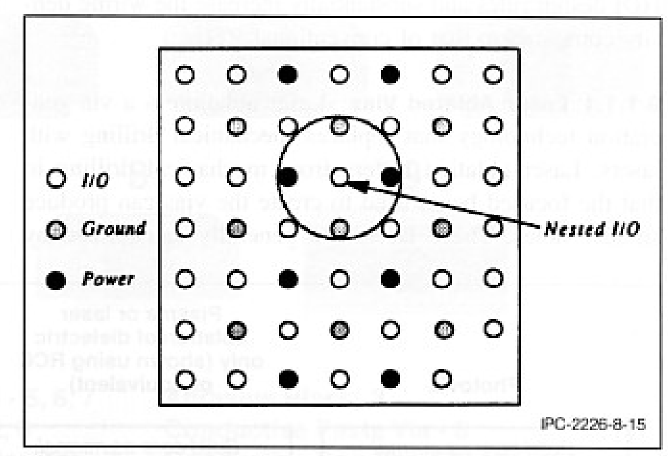


Figure 8-15 Nested I/O Footprint

9 HOLES/INTERCONNECTIONS

The general requirements for holes, lands, minimum annular ring and standard fabrication allowances related to the core material, as well as surface-to-surface PTHs, are referenced in IPC-2221, IPC-2222 and IPC-2223.

This section deals specifically with the requirements for HDI layers.

9.1 Microvias

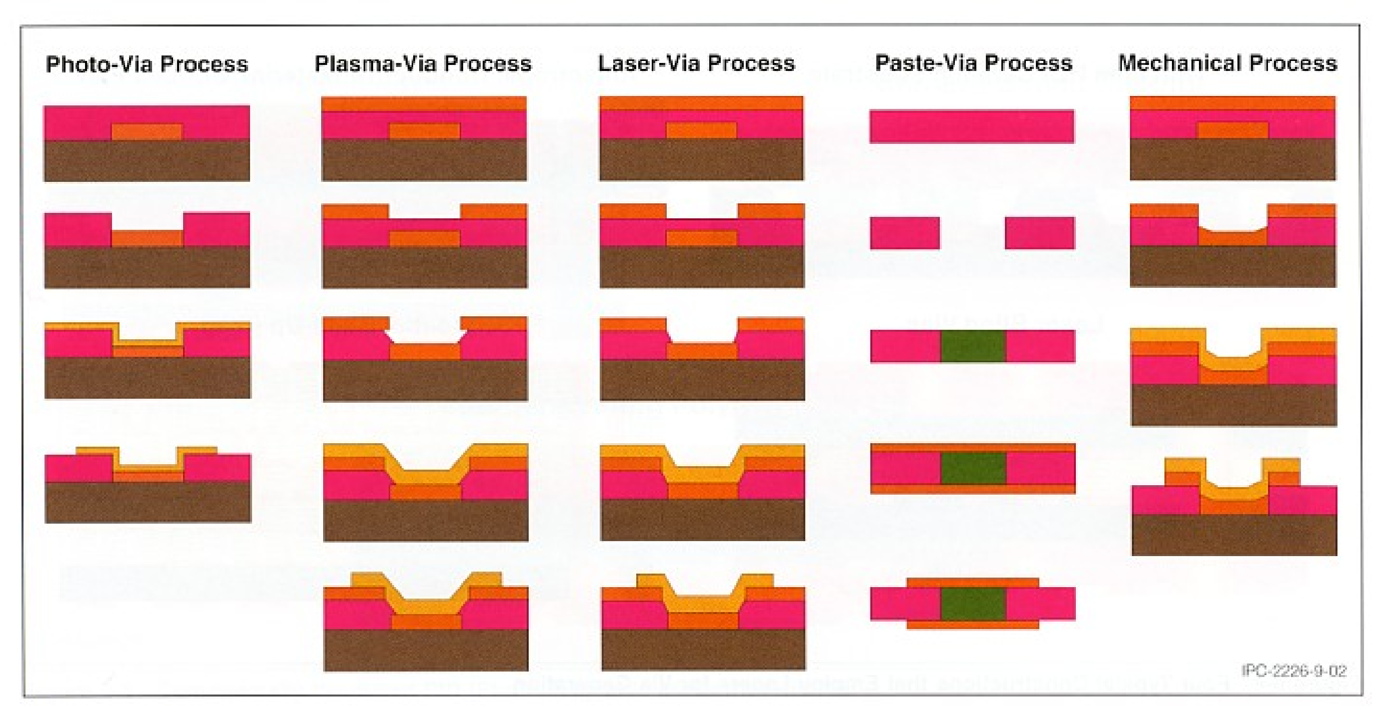


Figure 9-2 Microvia Manufacturing Processes

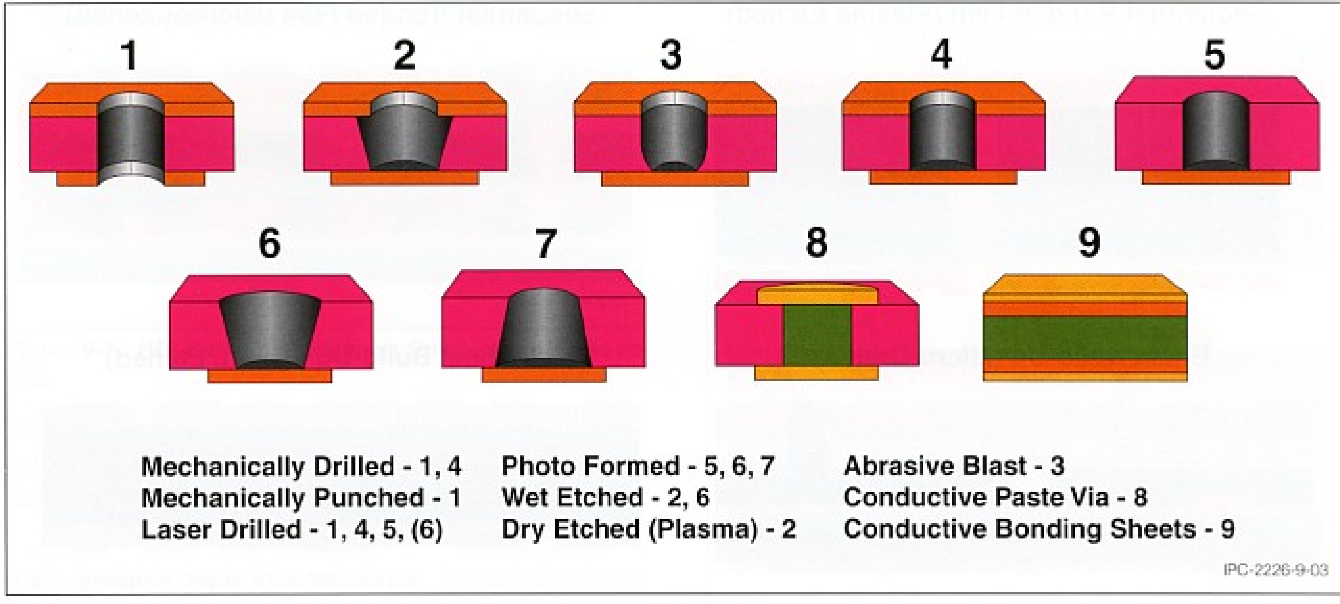


Figure 9-3 Cross-Sectional Views of Methods to Make HDI with Microvias

and/or plugged holes. Microvias are formed by photoimaging. A layer of dielectric is coated over the base substrate. The microvias or circuit paths are imaged, developed, cured and subsequently metallized to allow for patterning.

First used in 1988, the photoimageable dielectric was a modified solder mask. Today, modern photoimageable dielectrics (PID) are optimized as a dielectric in liquid or dry film format and can be positive or negative acting. This is also a mass (global) via generation technique, forming all vias in a single operation.

9.1.1.4 Conductive Inks/Insulation Displacement Figure 9-7 shows a dielectric layer with microvias formed by photo-imaging, laser or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished by either laminating copper foil onto the dielectric surface or by chemical deposition.

9.2 Via Interconnect Variations

9.2.1 Stacked Microvias When one or more microvias are vertically aligned and interconnected with another microvia, the result is a set of stacked microvias. Figure 9-8 shows different types of stacked microvias.

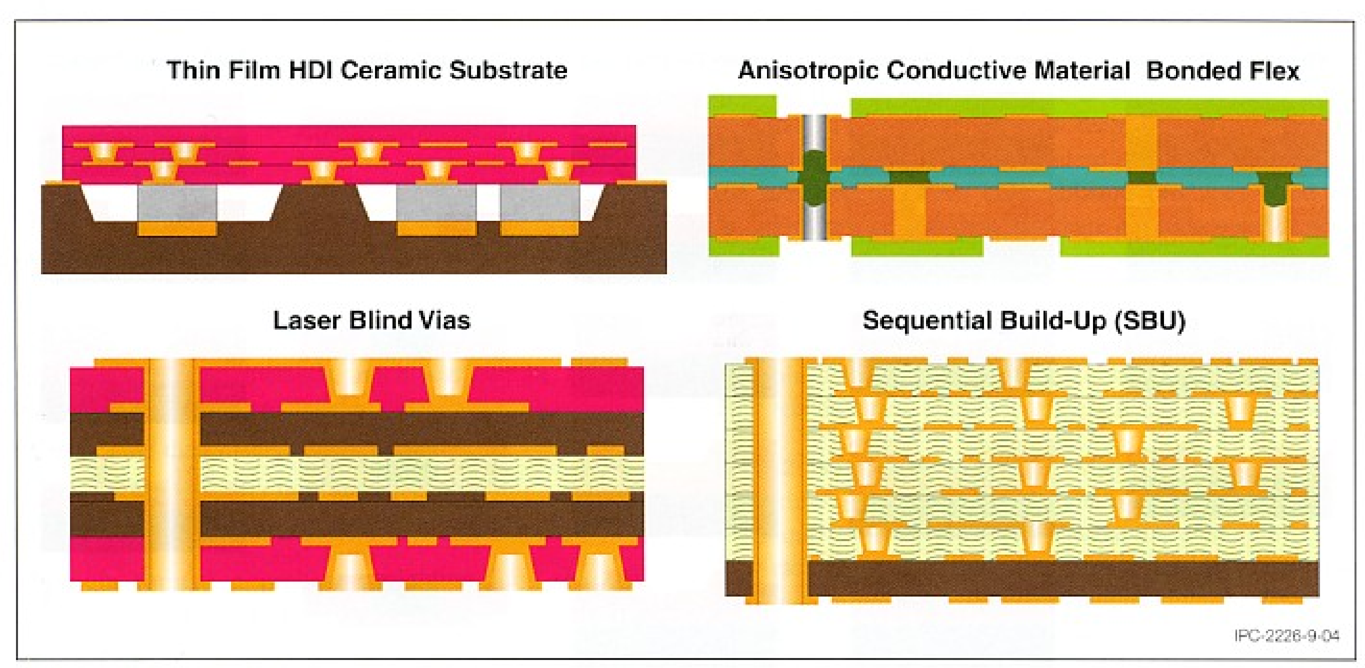


Figure 9-4 Four Typical Constructions that Employ Lasers for Via Generation

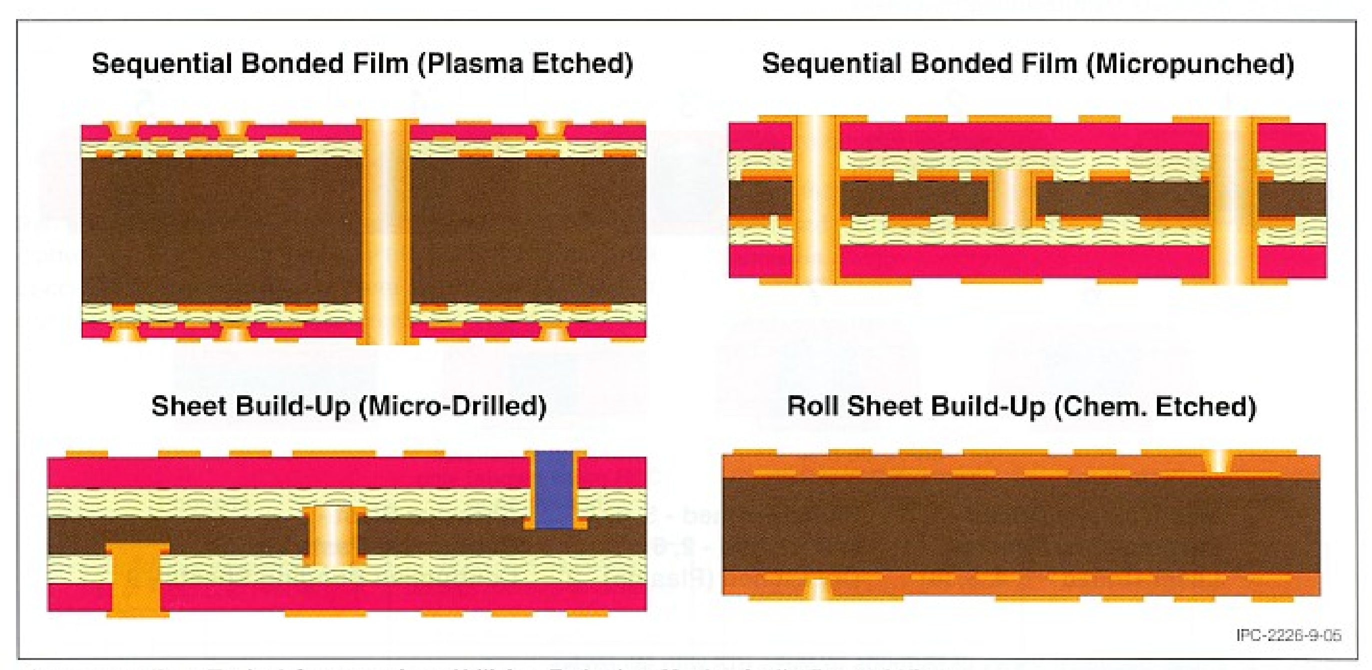


Figure 9-5 Four Typical Constructions Utilizing Etched or Mechanically Formed Vias

9.2.2 Stacked Vias When one or more microvias are vertically aligned and interconnected with a buried via, the result is a set of stacked vias. Figure 9-9 shows different types of stacked vias.

9.2.3 Staggered Microvias A staggered microvia is formed when one or more microvias interconnect in a manner such that the target pad of one microvia is tangential or greater to the capture pad of the subsequent microvia (see Figure 9-10).

NOTE: Violating the tangency requirements when designing staggered microvias may violate annular ring requirements and reduce reliability.

9.2.4 Staggered Vias A staggered via is formed when a microvia and buried via interconnect in a manner such that the target pad of the microvia is tangential or greater to the capture pad of the subsequent buried via. The microvia may be connected to other microvia combinations (see Figure 9-10). Figure 9-11 shows an isometric view of a staggered microvia.

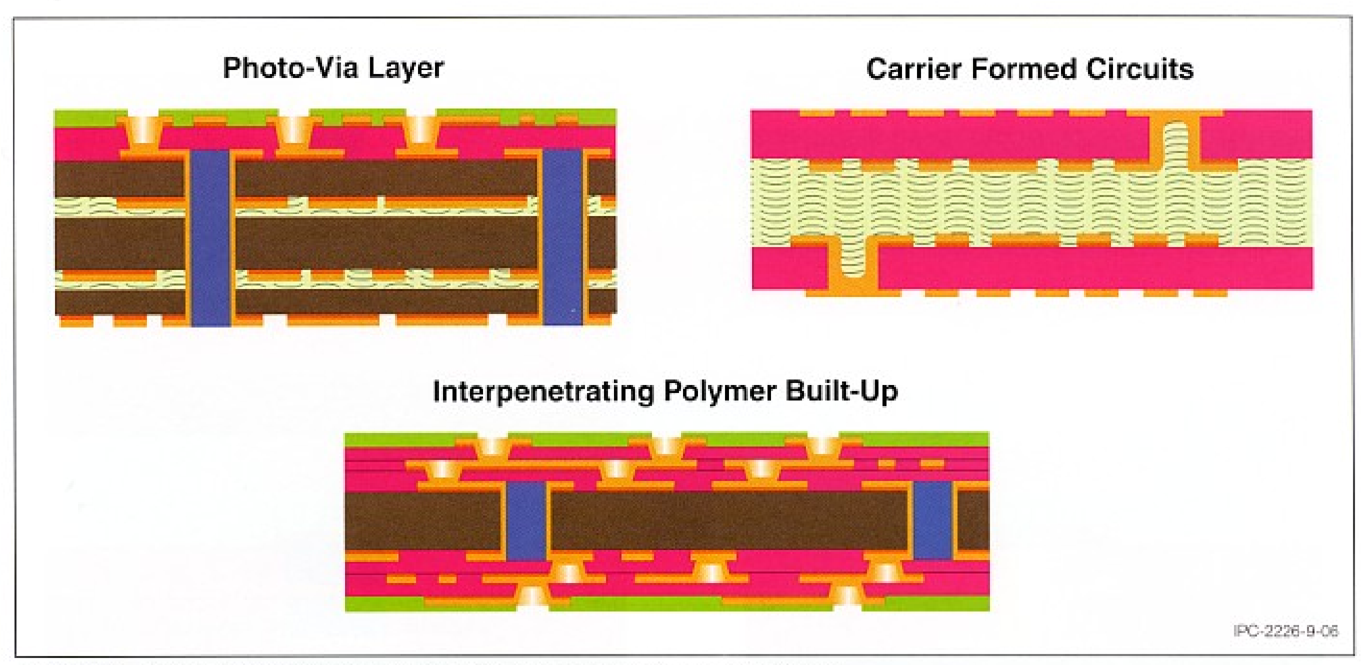


Figure 9-6 Commercially Produced PID (Photoimageable Dielectric) Boards

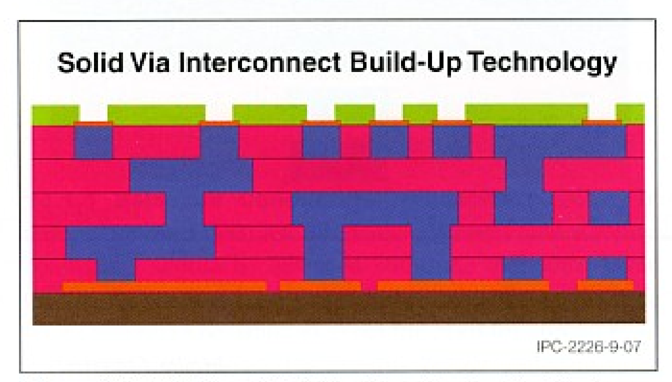


Figure 9-7 HDI Board that Employs Conductive Pastes as Vias

NOTE: Violating the tangency requirements when designing staggered vias may violate annular ring requirements and reduce reliability.

9.2.5 Variable Depth Vias/Microvias Variable depth vias and microvias are formed in one process step, penetrating two or more HDI dielectric layers and making connection between two or more layers. When a variable depth via passes through any given layer without making a connection, a clearance hole (anti-pad) is required.

It should be noted that the depth of the hole should not increase the plating aspect ratio beyond the manufacturing capabilities of the circuit board fabricator.

Figure 9-12 displays various variable depth vias.

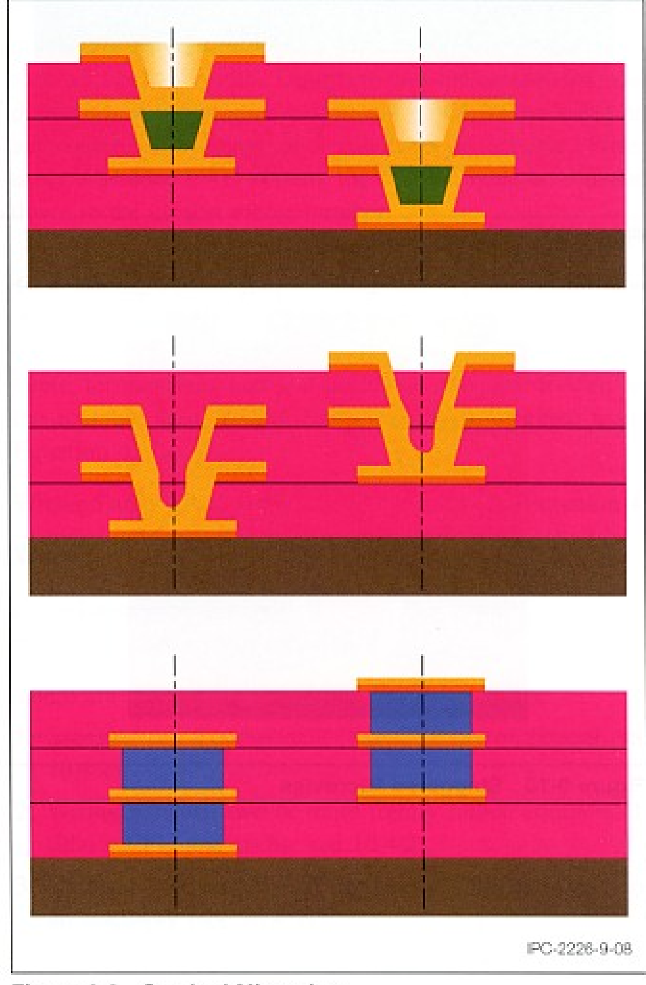


Figure 9-8 Stacked Microvias

IPC-2226-9-09

Figure 9-9 Stacked Vias

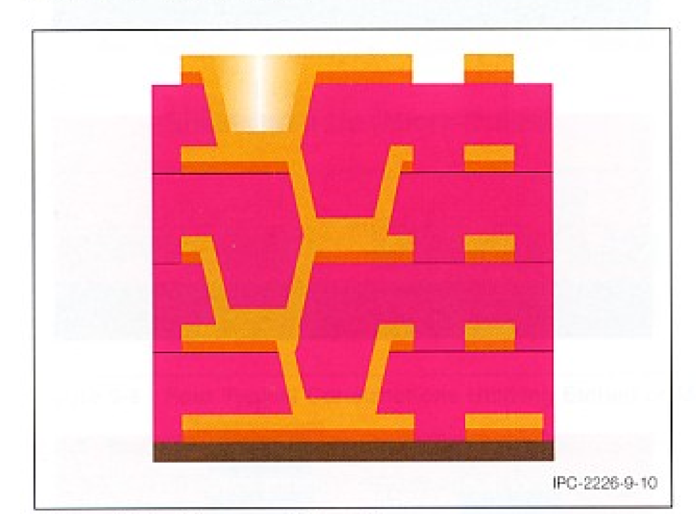


Figure 9-10 Staggered Microvias

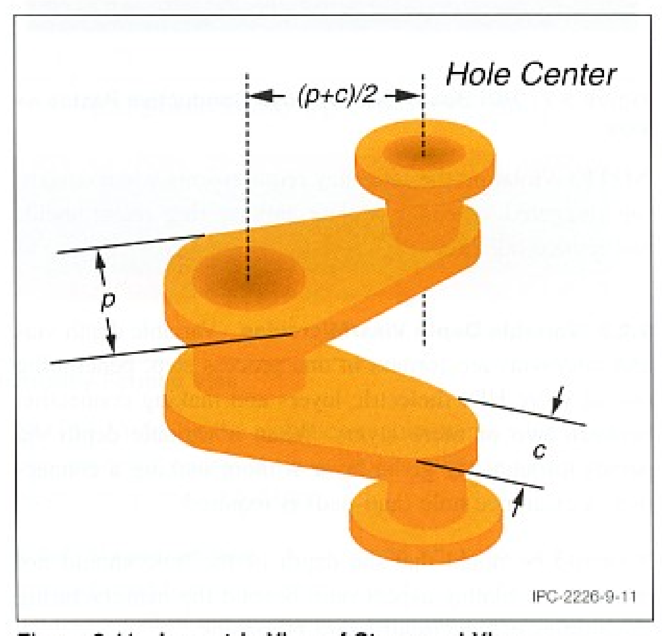


Figure 9-11 Isometric View of Staggered Vias

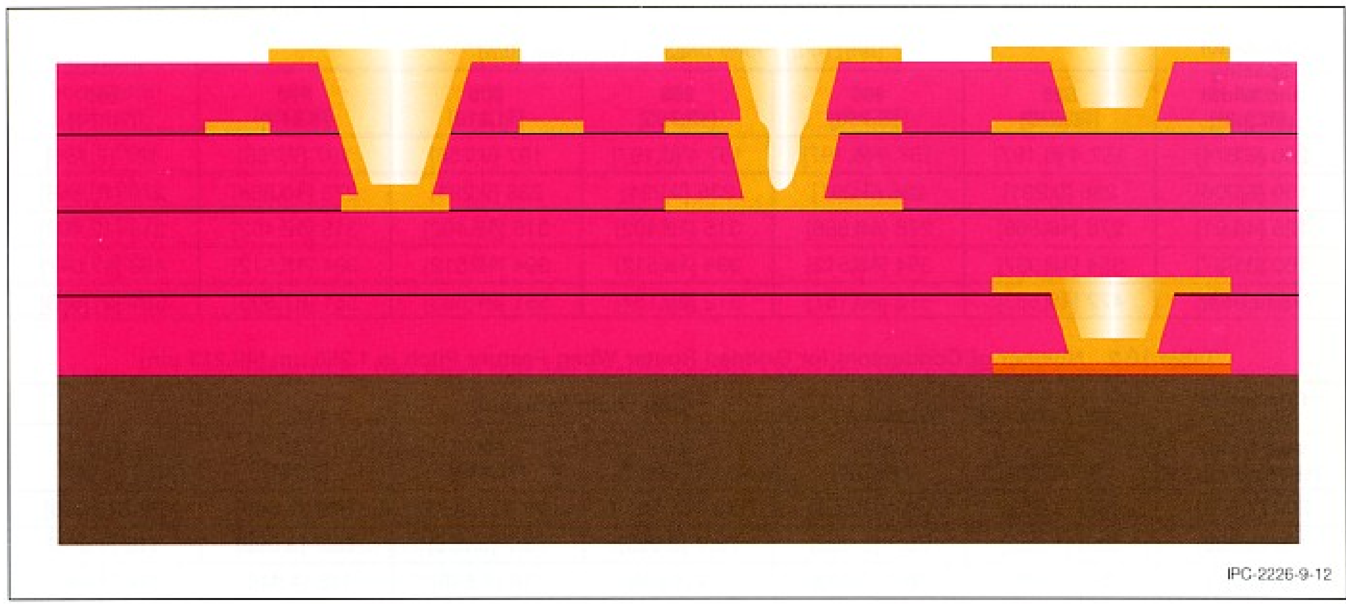


Figure 9-12 Variable Depth Vias/Microvias

10 GENERAL CIRCUIT FEATURE REQUIREMENTS

10.1 Conductor Characteristics Conductor characteristics **shall** be in accordance with the generic standard IPC-2221 and as follows:

10.1.1 Balanced Conductors Whenever possible, to reduce bow and twist and to increase dimensional stability, conductors should be balanced within an individual layer. Conductor routing density should be spread throughout the board wherever possible, to avoid the need for special etching or plating thieves. Plating thieves are added metallic areas, which are nonfunctional on the finished board but allow uniform plating density, giving uniform plating thickness over the board surface.

10.2 Land Characteristics Land characteristics **shall** be in accordance with IPC-2221.

10.3 Determining the Number of Conductors Use Equation 2 to determine the number of conductors that can be used based on feature pitch.

Number of Conductors $(C_N) = (F_P - L_D - 2_s + C_S) / C_W + C_S)$ [Equation 2]

When $C_S = S$, the equation simplifies to Equation 3.

$C_N = [F_P - L_D - C_S]/(C_W + C_S)$ [Equation 3]

Where:

F_P = Feature pitch
L_D = Land diameter
C_S = Conductor spacing
C_W = Conductor width
s = Spacing between conductor and land

Table 10-1, Table 10-2, Table 10-3, Table 10-4 and Table 10-5 cover various feature pitch, land diameters and conductor widths and spacings and give the number of conductors per channel width. Designers can interpolate for land diameters and line/space widths not listed. When using an autorouter, the fraction of a conductor is useable. When using a gridded CAD system, the fraction must be rounded down to the closest whole number.

10.4 Wiring Factor (Wf) Wiring factor is the actual density of a board resulting from the wiring distance required to connect all the electrical terminations of all the components, terminations and test points on a board divided by the routable area. Wiring factor can be determined using Equation 4.

Wiring Factor $(W_F) = \varepsilon W_C$ [Equation 4]

Where:

ε = Layout efficiency
W_C = Substrate wiring capacity

There are three cases that drive the wiring factor:

1. Escape from a component (like CSP or component; see 10.4.1).
2. Wiring between two or more tightly linked components (like a CPU and cache; see 10.4.2).
3. Demand produced by all components on both sides of an assembly (see 10.4.3).

10.4.1 Localized Escape Calculations Component land patterns can be peripheral or full array. Peripheral arrays are the most practical for using leading edge HDI design rules.

Table 10-1 Number of Conductors for Gridded Router When Feature Pitch is 2,500 µm [98,425 µin]

Conductor Spacing and Width µm [µin]	Land Width µm [µin]					
	525 [20,670]	400 [15,750]	350 [13,780]	300 [11,810]	250 [9,843]	200 [7,874]
200 [7,874]	157.4 [6,197]	157.4 [6,197]	157.4 [6,197]	197 [7,756]	197 [7,756]	197 [7,756]
150 [5,906]	236 [9,291]	236 [9,291]	236 [9,291]	236 [9,291]	276 [10,866]	276 [10,866]
125 [4,921]	276 [10,866]	276 [10,866]	315 [12,402]	315 [12,402]	315 [12,402]	315 [12,402]
100 [3,937]	354 [13,937]	394 [15,512]	394 [15,512]	394 [15,512]	394 [15,512]	433 [17,047]
75 [2,953]	472 [18,583]	512 [20,157]	512 [20,157]	551 [21,693]	551 [21,693]	551 [21,693]

Table 10-2 Number of Conductors for Gridded Router When Feature Pitch is 1,250 µm [49,213 µin]

Conductor Spacing and Width (µm) [µin]	Land Width (µm) [µin]					
	525 [20,670]	400 [15,750]	350 [13,780]	300 [11,810]	250 [9,843]	200 [7,874]
200 [7,874]	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	78.7 [3,098]	78.7 [3,098]
150 [5,906]	39.4 [1,551]	78.7 [3,098]	78.7 [3,098]	78.7 [3,098]	78.7 [3,098]	118 [4,646]
125 [4,921]	78.7 [3,098]	78.7 [3,098]	118 [4,646]	118 [4,646]	118 [4,646]	118 [4,646]
100 [3,937]	118 [4,646]	118 [4,646]	157.4 [6,197]	157.4 [6,197]	157.4 [6,197]	157.4 [6,197]
75 [2,953]	157.4 [6,197]	197 [7,756]	197 [7,756]	197 [7,756]	236 [9,291]	236 [9,291]

Table 10-3 Number of Conductors for Gridded Router When Feature Pitch is 650 µm [25,591 µin]

Conductor Spacing and Width (µm) [µin]	Land Width (µm) [µin]					
	525 [20,670]	400 [15,750]	350 [13,780]	300 [11,810]	250 [9,843]	200 [7,874]
200 [7.874]	NA	NA	NA	NA	NA	NA
150 [5.906]	NA	NA	NA	NA	NA	39.4 [1,551]
125 [4.921]	NA	NA	NA	NA	39.4 [1,551]	39.4 [1,551]
100 [3.937]	NA	NA	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]
75 [2.95]	NA	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	78.7 [3,098]	78.7 [3,098]

Table 10-4 Number of Conductors for Gridded Router When Feature Pitch is 500 µm [19,685 µin]

Conductor Spacing and Width (µm) [µin]	Land Width (µm) [µin]					
	400 [15,750]	350 [13,780]	300 [11,810]	250 [9,843]	200 [7,874]	150 [5,906]
200 [7,874]	NA	NA	NA	NA	NA	NA
150 [5,906]	NA	NA	NA	NA	NA	NA
125 [4,921]	NA	NA	NA	NA	NA	NA
100 [3,937]	NA	NA	NA	NA	39.4 [1,551]	39.4 [1,551]
75 [2,953]	NA	NA	NA	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]
50 [1,969]	NA	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]	39.4 [1,551]

10.4.1.1 Full Array Equation 5 can be used for predicting the number of signal layers for breakout of a particular group of I/Os on a component as seen below.

Number of Signal Layers =

$$[[n / 2] - [(G - D_B - C_S) / (C_W + C_S)] + 1 / [(G - D_V - C_S) / (C_W + C_S)] + 1]_{INT} + 1 \quad \text{[Equation 5]}$$

Where:

C_W = Conductor width

C_S = Conductor spacing

D_V = Capture land diameter

D_B = Target land diameter

G = I/O pitch

n = Number of rows in full square array

10.4.1.2 Peripheral Array The general equation for peripheral array components is similar to that for area array. It requires only the substitution of the term 'r' (r = the number of rows deep of contacts) for the n/2 term in Equation 5. The chip or package will be larger than a full array, but the design rules and number of signal layers will be much less aggressive.

Table 10-6 displays the number of pad rows that can escape from a full or peripheral array component per HDI layer

Table 10-5 Number of Conductors for Gridded Router When Feature Pitch is 250 µm [9,843 µin]

Conductor Spacing and Width (µm) [µin]	Land Width (µm) [µin]					
	350 [13,780]	300 [11,810]	250 [9,843]	200 [7,874]	150 [5,906]	100 [3,937]
150 [5,906]	NA	NA	NA	NA	NA	NA
125 [4,921]	NA	NA	NA	NA	NA	NA
100 [3,937]	NA	NA	NA	NA	NA	NA
75 [2,953]	NA	NA	NA	NA	NA	NA
50 [1,969]	NA	NA	NA	NA	NA	39.4 [1,551]

Table 10-6 Pad Rows that can Escape per HDI Layer for Different Feature Sizes

Trace/Space (µm) [µin]	Pad Diameter (cm) [in]	Component Pitch Size (mm) [in]					
		1.15 [0.04528]	1.0 [0.0394]	0.80 [0.0315]	0.75 [0.0295]	0.65 [0.0256]	0.50 [0.0197]
75 [2,953]	0.025 [0.009842]	6	5	4	3	3	2
	0.030 [0.01181]	6	5	3	3	2	1
	0.035 [0.01378]	5	4	3	3	2	1
	0.040 [0.01575]	5	4	3	2	2	1
100 [3,937]	0.025 [0.009842]	4	4	3	2	2	1
	0.030 [0.01181]	4	3	2	2	2	1
	0.035 [0.01378]	4	3	2	2	1	1
	0.040 [0.01575]	4	3	2	2	1	1
125 [4,921]	0.025 [0.009842]	4	3	2	2	2	1
	0.030 [0.01181]	3	3	2	2	1	1
	0.035 [0.01378]	3	3	2	2	1	1
	0.040 [0.01575]	3	2	2	1	1	1

using blind microvias. If the chip and substrate size of a peripheral array can be accommodated, the reduced design rules and layer count has a beneficial effect on PCB fabrication costs.

10.4.2 Wiring Between Tightly Linked Components Equation 6 shows how to calculate tightly linked components or the substrate wiring capacity WC.

$$W^C = ((2.5) * (N_T) * (P_N -1) * R) / ((P) * (P_N) * (\varepsilon)) \quad \text{[Equation 6]}$$

Where:

N_T = Number of I/O per component

P_N = Leads per net

ε = Wiring efficiency (30% to 80%)

P = Module pitch

R = Average wiring length = $(k * (1 + 0.1\ln N) * N^{1/6})$ - k = 0.75

N = Number of components

Figure 10-1 gives a visual example of this equation. An alternate equation can be used to give a close approximation. The wiring factor (cm/cm^2) [in/in sq.] can now be determined using Equation 7.

$$W_C = (2.25\ N_T) / P \quad \text{[Equation 7]}$$

Where:

N_T = Number of I/O per component

P = Pitch between active components

Dr. Donald Seraphim, IBM, made such a derivation (based on an empirical analysis) and observed that it is impossible to fill all available wiring channels with conductors. The empirically established efficiency, ε, is between 25% and 70%. Fifty percent efficiency is normally used, thus the maximum available wiring capacity (connectivity) must be twice the length of the necessary or actually required wiring (wiring factor).

10.4.3 Total Wiring Requirements As a general rule, the escape routing from microcomponents does not exclusively determine the design rules or number of signal layers.

Other factors such as the printed wiring assembly form factor, the pitch of the other SMT components, how many parts are on the back side and the distance between parts may drive the need for different design rules and more signal layers than those required by the pin out of the microcomponents alone.

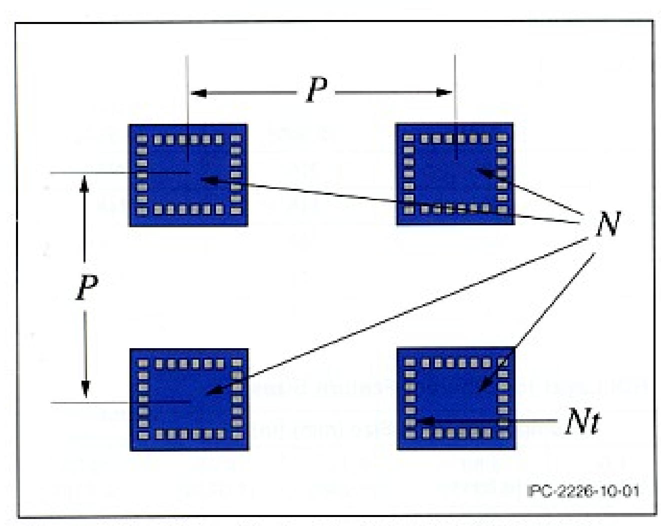


Figure 10-1 Wiring Factor Model for Tightly Coupled Components

The easiest equation to use is the wiring density (W D) predictor given in Equation 8, which relates to the total parts on both sides of an assembly, the assembly area, total number of leads and a factor relating the semiconductor technology being used.

$$W_D = \beta\sqrt{(p/a)}\bullet(l/p) \qquad \text{[Equation 8]}$$

Where:

p = Total parts on both sides of an assembly

a = Area on an assembly (one surface only)

l = Total leads of all parts including connector fingers

β = 2.5 (analog & digital, high discrete)

β = 3.0 (digital products)

β = 3.5 (high ASIC focus, MCM, PCMCIA)

This wiring density (W_D) predictor is the actual wiring in cm/cm^2 that an average of three nodes per net would require for the parts (p) with leads (l) on a PCB area (a).

This is related in the equation for wiring factor (see Equation 4).

To convert the wiring factor into a series of layer count and design rule combinations that will satisfy the density requirements of the proposed HDI design, the PCB layout system efficiency is divided into the wiring factor. PCB CAD layout efficiency is estimated from benchmarking actual designs and is only an approximation. Each designer, CAD system and placement methodology will affect the routing efficiency.

Table 10-7 shows the estimated efficiencies (e) that can be used for various design combinations.

10.5 Via and Land Density Higher via density conflicts with higher conductor density. However, it is not the via itself that causes the conflict; it is the land required for the via. This is because the capture land and conductor pattern occupy the same routing surface on the layer. The land is the locus of position the via could have considering all the

Table 10-7 Efficiencies

Design Scenario	Conditions	Efficiency (E) (%)
Normal Rigid	Through-hole SMT with/ without back side passives (gridded CAD)	25
Normal Rigid	Through-hole SMT with/ without back side passives (gridded CAD)	45
Normal Rigid	Through-hole SMT with back side active component (gridded CAD)	40
Normal Rigid	One side blind vias (using autorouter)	60
Normal Rigid	Two side blind vias (using autorouter)	70
Two-Layer Redistribution	Using autorouter	75
Four-Layer Redistribution	Using autorouter	80

fabrication and material tolerances. So the via can become increasingly smaller and the land will still be needed, a compromise must exist between the number of via/land sites on the PCB and the conductor density.

For example, a feature pitch of 1.25 mm [0.04921 in] permits a maximum of 64 vias/cm^2 [163 vias/in^2], a pitch of 0.65 mm [0.0256 in] permits 225 vias/cm 2 [572 vias/in^2] and a pitch of 0.50 mm [0.0197 in] permits 400 vias/cm^2 [1016 vias/in^2].

10.6 Trade Off Process

10.6.1 Wiring Factor Process Figure 10-2 gives an example of a wiring process flow chart.

10.6.2 Input/Output (I/O) Variables The input variables for the trade off formulas are given in Equation 9, Equation 10, Equation 11, Equation 12, Equation 13 and Equation 14.

Parts per square area (PPA) = p / s [Equation 9]

Average leads per part (LPP) = l / p [Equation 10]

$W_D = 3.5 * (\sqrt{PPA}) * LPP$ [Equation 11]

$W_C = W_D / P_L$ [Equation 12]

Where:

P_L = PCB layout efficiency - The percentage of wiring capacity the wiring factor consumes.

Number of layers (L) = $(W_C * G) / C_N$ [Equation 13]

Where:

G = Channel width - The width of the space between adjacent via holes or component lands with which to run conductors.

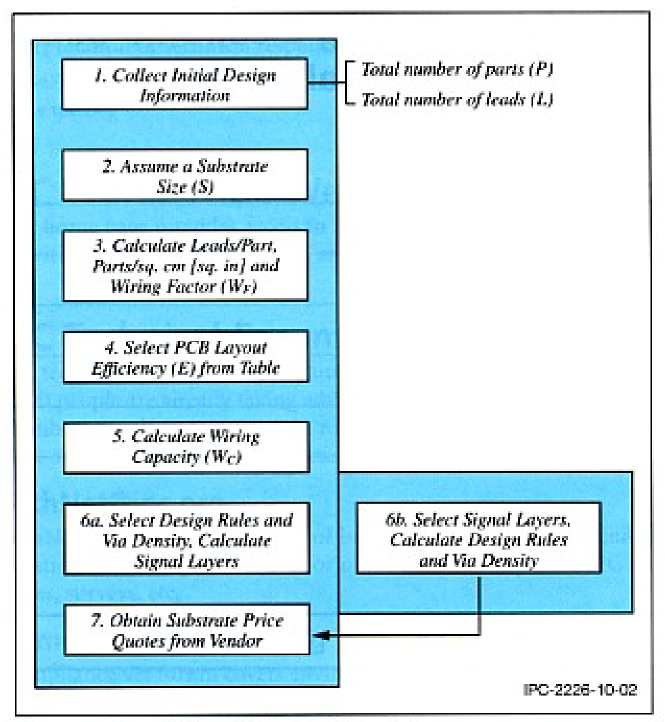


Figure 10-2 Wiring Process Flow Chart

Number of Conductors (C_N) = (W_C * G) / L [Equation 14]

Where:

L = Signal layers - The number of PCB layers dedicated to running conductors (does not include power or ground layers).

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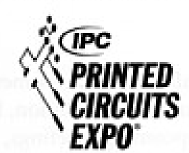
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